## High Side Switching and Inrush Limiting Using P Channel MOSFETs

P Channel MOSFETs are often used as high side switches due to the simple gate drive requirements. Such circuits were used on first generation notebook computers and hard drives in the early nineteen nineties. Fast forward to today and the availability of cost-effective 100-V and higher P-Channel MOSFETs with low on resistance allows their use for switching of 48-V and higher voltage rails with currents up to around ten Amps. Delays and inrush limiting can easily be accomplished in addition to switching by adding only three or four external passive components, making a very effective solution.

Figure 1 shows a high side switch and delay circuit. The switch, S1, could be implemented using a small signal MOSFET to allow control by a microcontroller, a shorter pin on a connector to enable the MOSFET after the power connections have been made, or even omitted completely (connect R2 to ground) to provide a delayed-action switch that can be designed to turn on a preset time after power is applied either for power sequencing or a simple hot swap circuit.

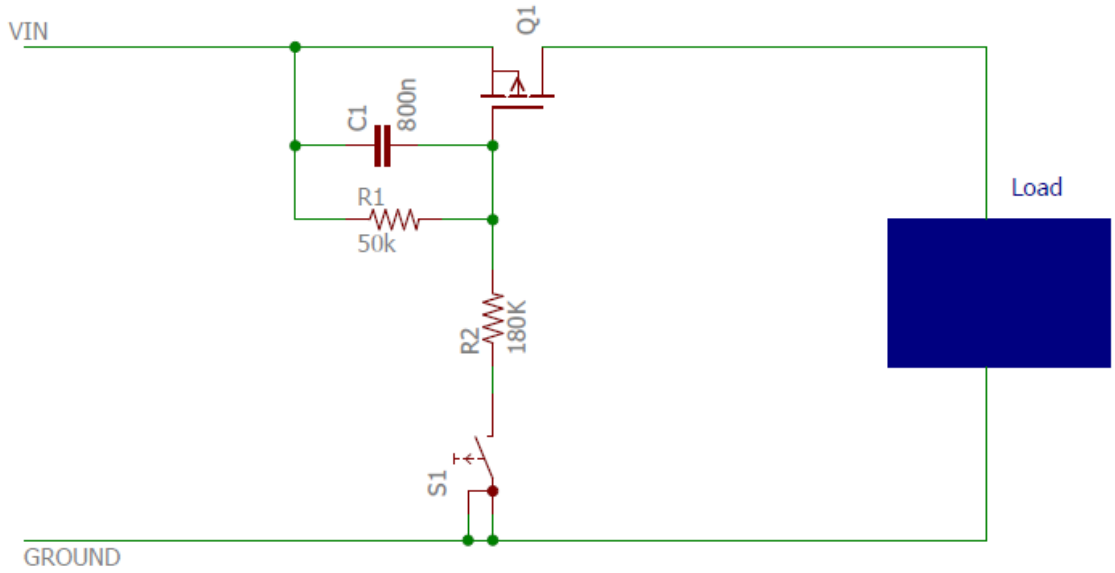


**Figure 1.** Simple High Side Switch with Delay.

C1, Gate to Source, is added mainly to create a delay, but it also has a small effect on the switching time, providing some inrush limiting. By adding a capacitor rather than simply using the MOSFET's CISS, the delay is much more consistent as it does not rely on the MOSFET's values. Using an external capacitor means that different part numbers can be used for the MOSFET with minimal effect on the timing.

The delay is best calculated using Thevenim to obtain a DC $V_{GS}$ on voltage and equivalent series resistance as shown in Figure 2.

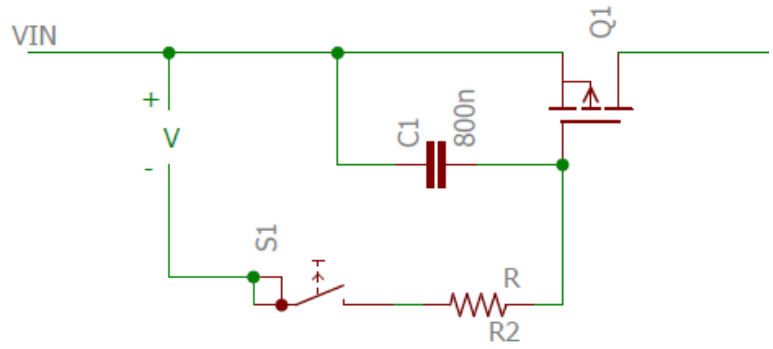


**Figure 2.** Thevenim Applied to the Gate Drive Circuit.

Assume VIN = 48V

V = 50/(50+180 ) x 48 = 10.4V

R = 50 x 180 / (50 + 180) = 39K Ohm

Assume the MOSFET begins to turn on at 1.5V as the lowest/fastest value.

Determine the number of time constants this equals, ($0.37^X$)

1 - (1.5/10.4) = 0.86 = 0.37 ^ 0.15

So 1.5V will be reached in 0.15 time constants, $\tau$. This allows us to calculate C for a given required delay:

$\tau$ = R x C where R = resistance (Ω), C = Capacitance, (F)

For a given delay D, seconds:

D = 0.15 $\tau$

D = 0.15 (R x C)

C = D/(0.15 x R)

If required minimum delay D = 5 ms

C = 0.005 / (0.15 x 39 x $10^3$) C = 800 nF

However this is a simple example and includes no inrush limit. Further modeling of the circuit and analysis of inrush is best done using Spice. LT Spice is a free and easy to use version that is perfect adequate for this application. LT Spice includes some MOSFET models, but the models are not very complex nor editable, so a simple alternative is to include the MOSFET model as a Spice directive text in the schematic. To enable such models the MOSFET device prefix should be set to “X” in the properties as shown in Figure 3.

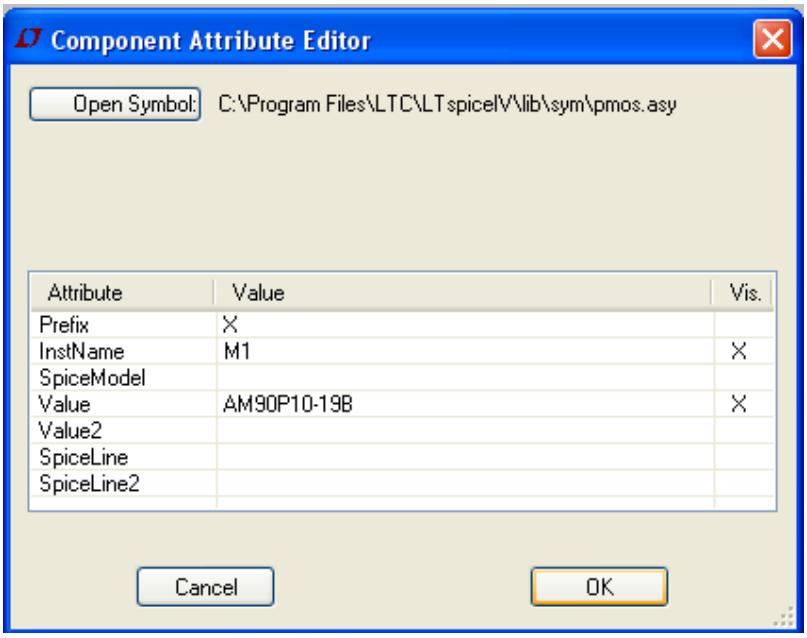


**Figure 3**. Properties of MOSFET with embedded model in LT Spice.

Figure 4 shows a LT Spice schematic for an AM90P10-19B on a 48V rail. A simplified Spice model for the AM90P10-19B is shown as a Spice directive in the schematic. The AM90P10-19B has a typical threshold voltage of about 3.2V, so the delay is just over twice what we calculated for in the above example. Note that this simple Spice model does not include increase in CRSS capacitance at lower $V_{DS}$ because we are going to add external capacitors to swamp the value of the MOSFET. The increase in capacitance at lower values of Drain-Source voltage is also not important here as the peak power occurs at high Drain-Source voltages. The switch is shown as a 2N7002 simply because it is a device included in LT Spice and Spice works better with devices with finite switching times rather than switches.

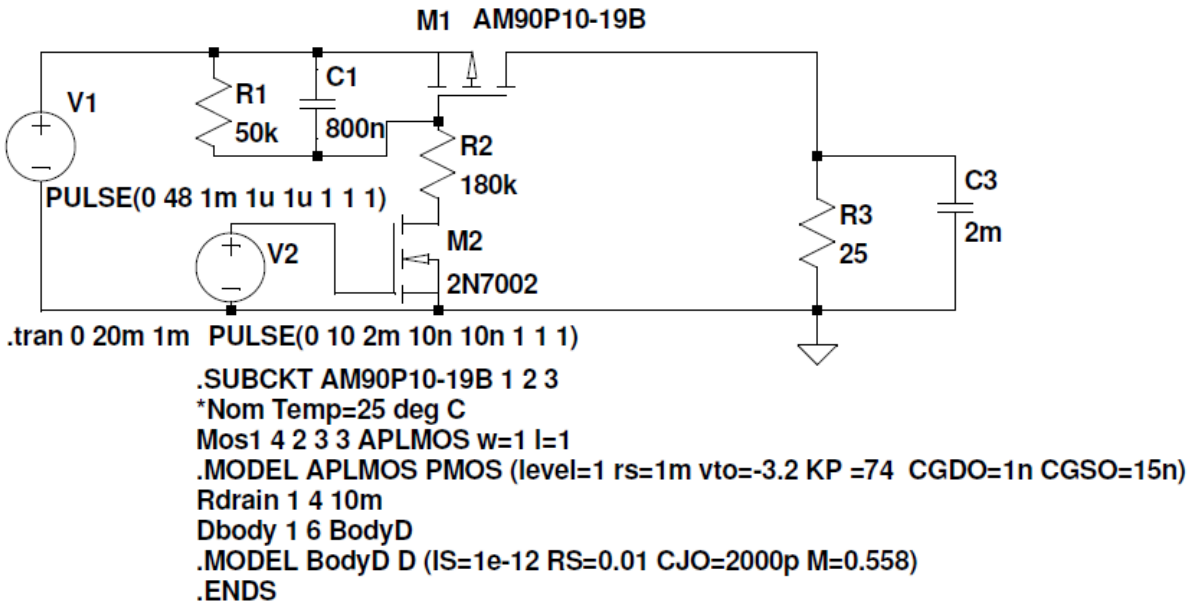


**Figure 4.** LT Spice Circuit for Basic Circuit in Figure 1.

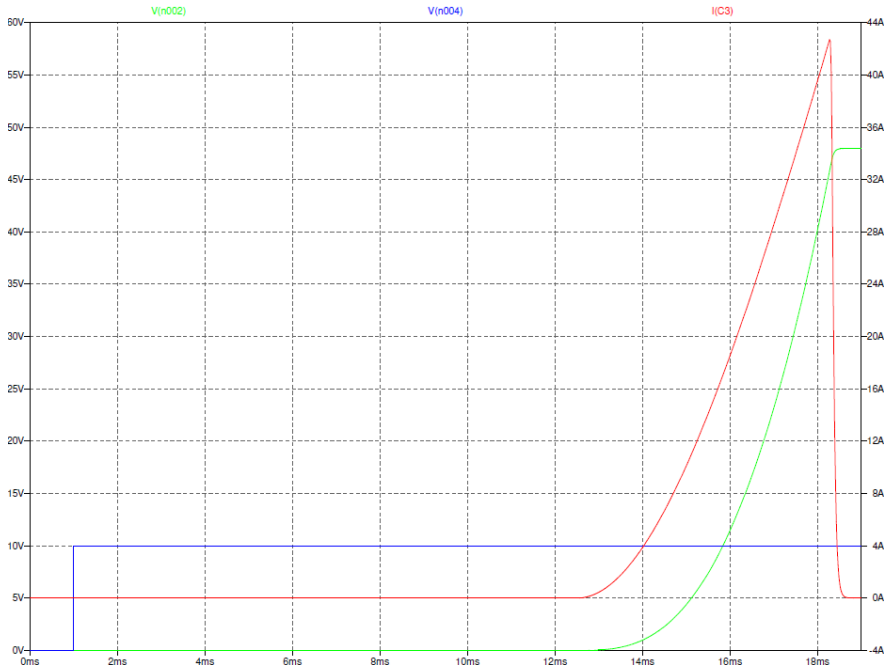


**Figure 5.** LT Spice Simulation Output for Circuit in Figure 4.

LT Spice shows a 12ms delay and a rise time of about 2 ms, about what we would expect. However this turn on time may be too short for a load with high capacitance as the dv/dt is about 40 V/ms, resulting in an excessive inrush current as shown here. With the ideal components used here and a 2 mF load, the peak current is approximately 45 A, however this is using a simple Spice model with no increase in capacitance as VDS decreases, so in practice it may be about half this value. The level of detail for this model was not intended to model inrush with no added capacitance from Gate to Drain.

The inrush current can be moderated by adding a capacitor from Gate to Drain, with a maximum value approximately 1 / the input voltage x the $C_{GS}$ to ensure that the capacitive divider formed by the two capacitors cannot provide a Gate-Source voltage that can allow the MOSFET to turn on. Capacitance added Gate to Drain will limit the dv/dt on the Drain, which is exactly what controls the inrush current for a load with high capacitance. Adding a 16 nFcapacitor from Gate to Drain gives the following result, the peak load current is just over 16A.

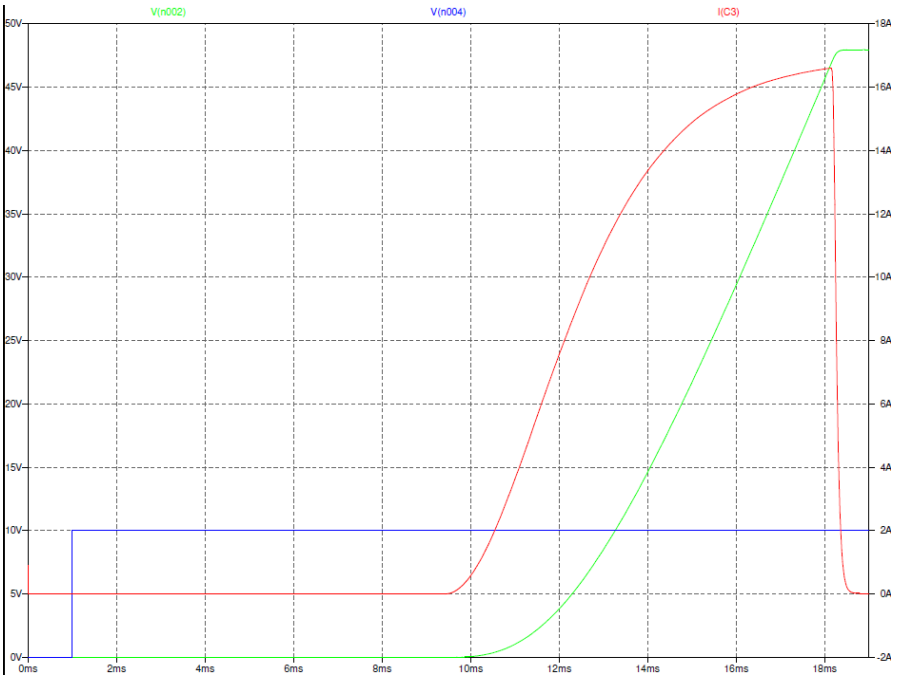


**Figure 6.** LT Spice Simulation For Schematic Shown in Figure 4, with 16nF connected Gate to Drain.

Since this inrush current is still too high, an example of 5uF Gate to Source and 100nF Gate to Drain is shown in Figure 7.

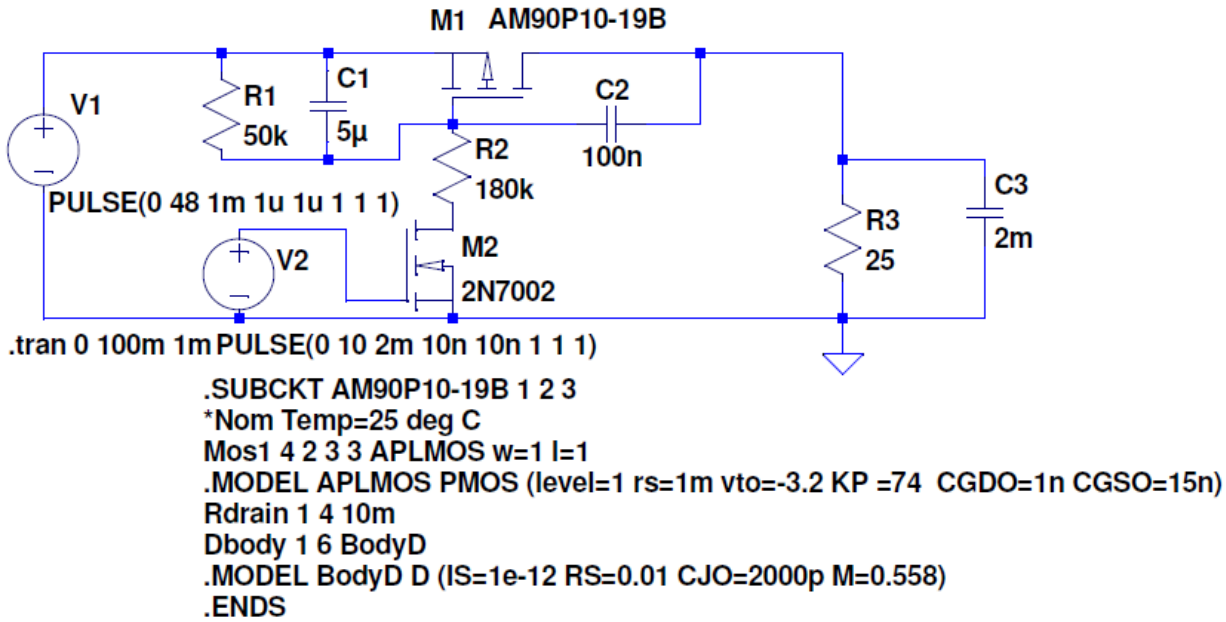


**Figure 7.** LT Spice Circuit for Lower Inrush current.

This yields the result shown in Figure 8, showing the inrush current is limited to about 3.25A

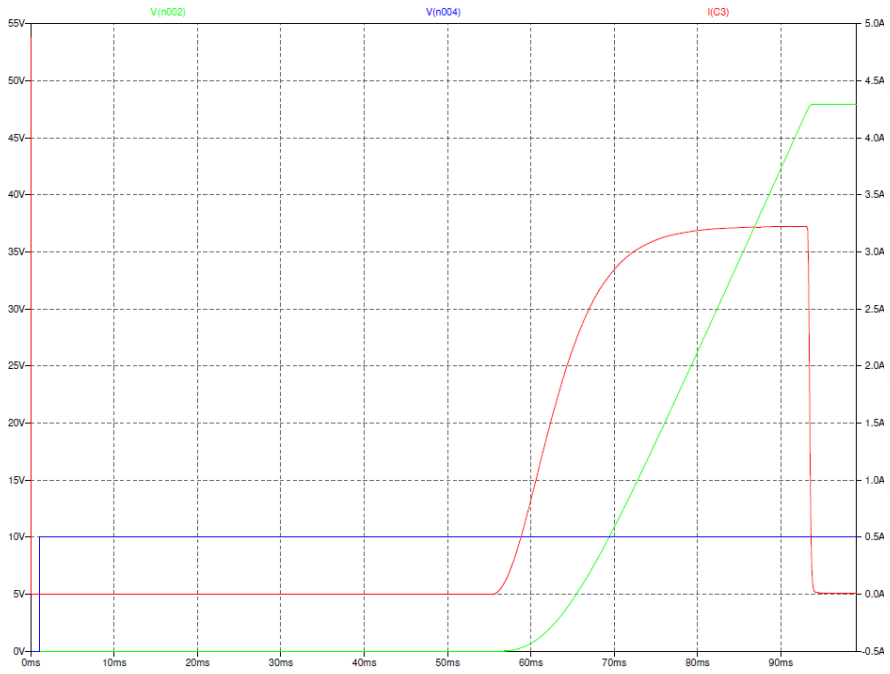


**Figure 8.** LT Spice Simulation for Improved / Lower Inrush Circuit in Figure 7.

Another simple way to look at this is that since the absolute value of the dv/dt over the load capacitance and the Gate-Drain capacitor is identical then the load capacitance inrush is given the following:

Assume VGS = 4V for switching (plateau voltage) to determine the current through the Thevenim equivalent resistance:

Current flowing through Thevenim R = (10.4 - 4 ) / 39K

= 0.16 mA

Current flowing onto 2mF load = Current through Gate-Drain Capacitor x $C_{Load}$ / $C_{GD}$

= 0.16 mA x 2 mF/100 nF

= 3.2 A

Therefore we can see that using Spice or the ratio of capacitances, it is easy to set a maximum dv/dt which in turn allows a maximum inrush current to be set. However care must also be observed to ensure that the SOA of the pass element is not exceeded, recognizing also that the SOA of the MOSFET may require to be derated.

The instantaneous power dissipated in the device equals the instantaneous voltage over the device multiplied by the current, it is a triangular pulse, peak value equal to $V_{IN}$ x $I_L$, where $V_{IN}$ is the input voltage and $I_L$ is the load current, and duration equal to the switching time of the circuit. Accurate calculation of temperature rise due to such power pulses using data sheet curves transient thermal impedance is cumbersome, and the easiest way is to use Spice for thermal modeling.

Analog Power can provide Spice thermal models based on Uniform Resistor Capacitor (URC) Spice components. The use of URC is much more accurate than lump values and allows segmenting the thermal resistance and capacitance to reflect actual physical parts of the device as opposed to several lump values that do not correspond to any distinct physical part of the package.

The Spice circuit is shown in Figure 9.

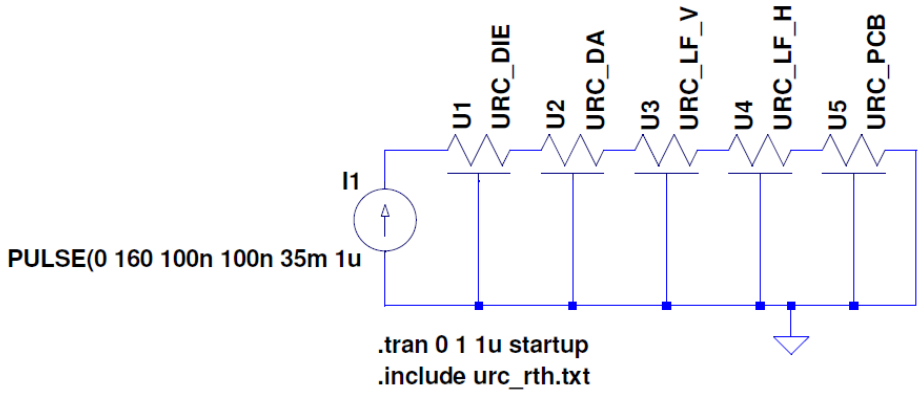


**Figure 9.** Analog Power Thermal Simulation Circuit in LT Spice.

To add values to the URC, the Spice directive .include urc_rth.txt is used and a text file of thqat name is placed in the same directory as the schematic of the form:

.MODEL URC_DIE urc(rperl=.2 cperl=25m)

.MODEL URC_DA urc(rperl=0.06 cperl=2.5m)

.MODEL URC_LF_V urc(rperl=0.48 cperl=0.0625)

.MODEL URC_LF_H urc(rperl=2 cperl=0.1375)

.MODEL URC_PCB urc(rperl=10 cperl=8)

Two MOSFETs will be considered with the following values

| Part | RDIE | CDIE m | RDA | CDA m | R_LF_Vert | C_LF_Vert | R_LF_Horiz | C_LF_Horiz | RPCB | CPCB |
|---|---|---|---|---|---|---|---|---|---|---|
| AM90P10-60B | 0.5 | 10 | 0.15 | 1 | 1.2 | 0.025 | 2 | 0.175 | 10 | 8 |
| AM90P10-19B | 0.2 | 25 | 0.06 | 2.5 | 0.48 | 0.0625 | 2 | 0.1375 | 10 | 8 |

The electrical/thermal power in Watts is represented in the circuit by a current in Amps. The above example of 3.25A for 35ms with $V_{IN}$ = 48V is represented by a current of 160A peak, triangular waveform falling to zero in 35 milliseconds, shown in blue in Figure 10.

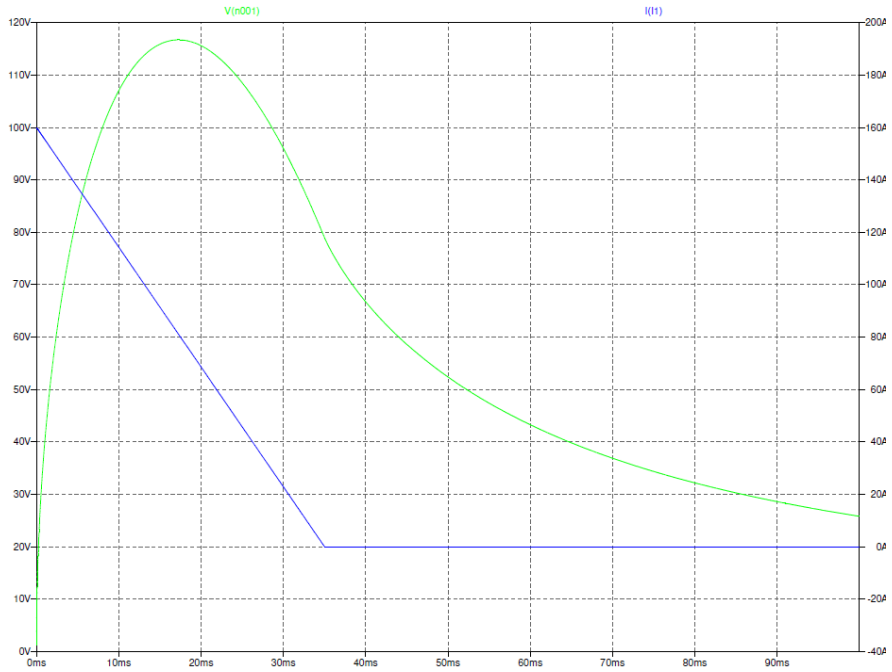


**Figure 10.** LT Spice Thermal Simulation Circuit Output for AM90P10-60B.

This shows a rise of about 117°C above the starting temperature. Arguably for 25°C ambient applications this would be acceptable. However we suggest a safe maximum junction temperature of 125°C to provide some derating since the MOSFET is operating below its Zero Temperature Coefficient and some regions of the die could be hotter than others due to local hotspot heating that can cause failures well within the devices maximum power dissipation[1]. Therefore even for 25°C ambient applications, the AM90P10-60B is not suitable with a 3.2A inrush for 35 ms.

Performing the same simulation for the AM90P10-19B, we get a rise of 47°C maximum, which would allow its use with ambient temperatures up to 80°C, suitable for most applications.

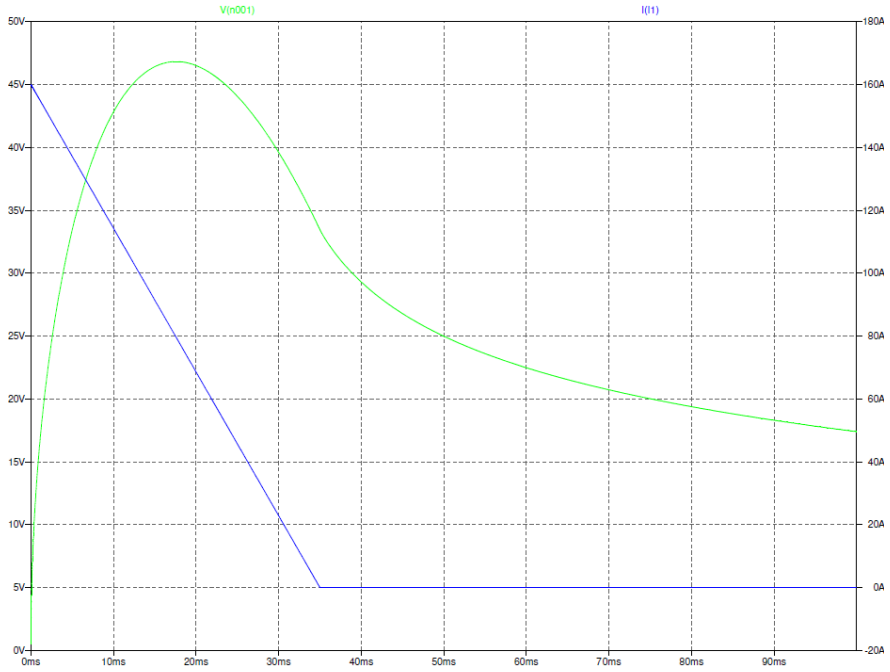


**Figure 11.** LT Spice Thermal Simulation Circuit Output for AM90P10-19B.

## Conclusion

P Channel MOSFETs make excellent high side switches and can be used for hot swap, power sequencing and inrush limiting. Use of a capacitor from Gate to Source will add a delay before turn on, and use of a capacitor from Gate to Drain will limit the dv/dt on the output of the switch which is the parameter that determines the inrush current of a capacitive load. Either Spice or simple calculations can be used to determine the capacitor values required for a given delay and or dv/dt. Since the power dissipated in the device is not a constant power pulse, calculation of temperature rise can be cumbersome and a Spice thermal model is the best solution. The SOA of a MOSFET used for applications such as current limit where the device is used in the saturated region (as opposed to the Ohmic region) can be significantly different to that predicted by the maximum power dissipation rating and therefore derating is suggested.

## References

1. Allan Cabiluna, YaFei Lv, ZhiPing Hu and Wonsuk Choi . AN4161 Practical Considerations of Trench MOSFET Stability when Operating in Linear Mode. Fairchild Semiconductor 2013-12-05