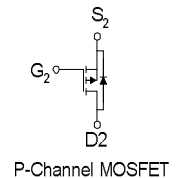
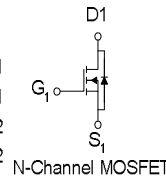
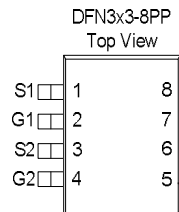


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	50 @ $V_{GS} = 10V$	5.8
	83 @ $V_{GS} = 4.5V$	4.5
-30	72 @ $V_{GS} = -10V$	-4.9
	105 @ $V_{GS} = -4.5V$	-4.0

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	20	-20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	5.8	-4.9	A
	$T_A = 70^\circ\text{C}$		4.8	-4	
Pulsed Drain Current ^b		I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a		I_S	2.9	-2.9	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	3.5	2.5	W
	$T_A = 70^\circ\text{C}$		2.2	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	35	$^\circ\text{C/W}$
	Steady State		85	$^\circ\text{C/W}$

Notes

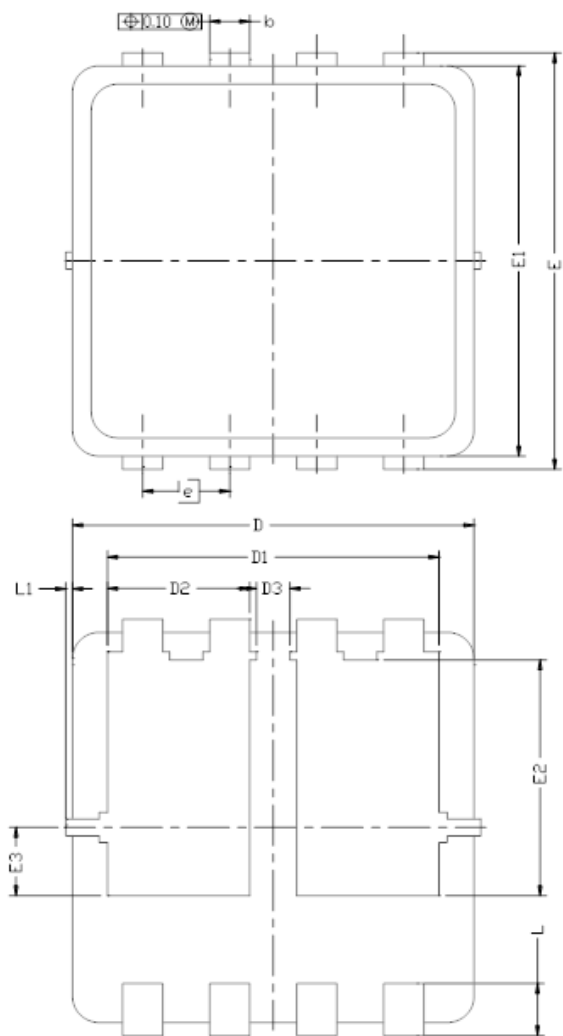
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25 ^o C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	1			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-1			
Gate-Body Leakage	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V	N			±100	nA
		V _{GS} = -20 V, V _{DS} = 0 V	P			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -10 V	P	-20			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 1 A	N			50	mΩ
		V _{GS} = 4.5 V, I _D = 1 A				83	
		V _{GS} = -10 V, I _D = -1 A	P			72	
		V _{GS} = -4.5 V, I _D = -1 A				105	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 1 A	N		40		S
		V _{DS} = -15 V, I _D = -1 A	P		31		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =1A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-1A	N		4		nC
Gate-Source Charge	Q _{gs}		P		8		
			N		1		
Gate-Drain Charge	Q _{gd}		P		2		
		N		1			
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =5V, I _D =1A , R _{GEN} =25Ω, P-Channel V _{DD} =-15V, V _{GS} =-5V, I _D =-1A R _{GEN} =15Ω	P		3		nS
			N		4		
P			5				
N			6				
Rise Time	t _r		P		7		
N				10			
Turn-Off Delay Time	t _{d(off)}		P		30		
N				5			
Fall-Time	t _f	P		10			

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.475 BSC			0.093 BSC		
D2	1.063 BSC			0.042 BSC		
D3	0.225 BSC			0.009 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.813 BSC			0.069 BSC		
E3	0.525 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
-	0?	10?	12?	0?	10?	12?