

P & N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

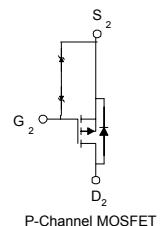
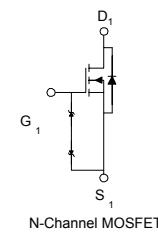
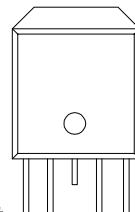
- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



**ESD Protected
2000V**

PRODUCT SUMMARY

V _{DS} (V)	r _{DS(on)} m(Ω)	I _D (A)
40	46 @ V _{GS} = 4.5V	28
	36 @ V _{GS} = 10V	33
-40	48 @ V _{GS} = -4.5V	-28
	38 @ V _{GS} = -10V	-33

**ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V _{DS}	40	-40	V
Gate-Source Voltage	V _{GS}	20	-20	
Continuous Drain Current ^a	I _D	33	-33	A
Pulsed Drain Current ^b	I _{DM}	±40	±40	
Continuous Source Current (Diode Conduction) ^a	I _S	30	-30	A
Power Dissipation ^a	P _D	50	50	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	-55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R _{θJA}	50	°C/W
Maximum Junction-to-Case	R _{θJC}	3.0	°C/W

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

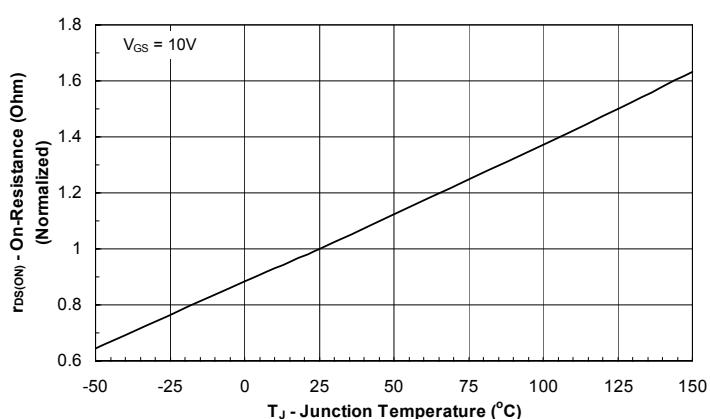
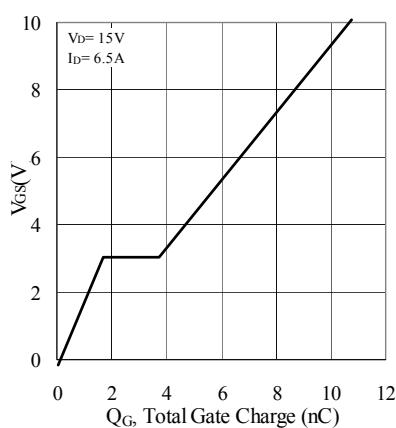
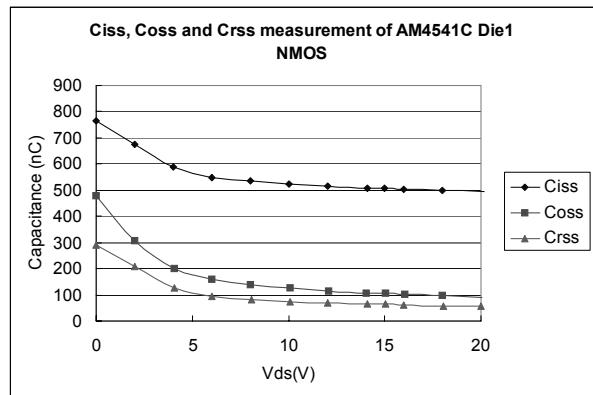
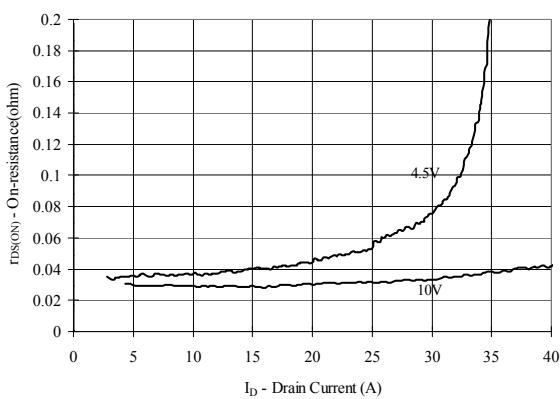
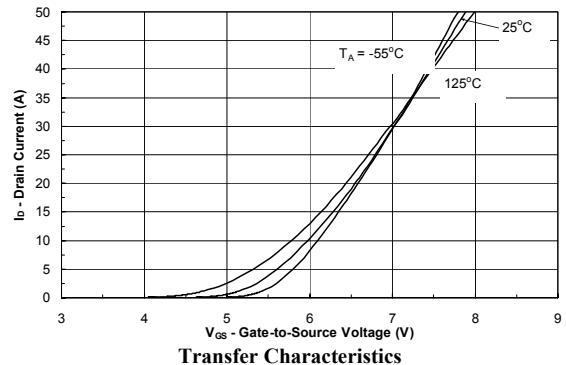
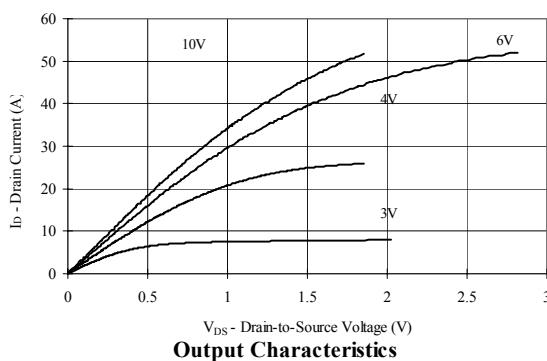
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	$V_{G(\text{th})}$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	N	1			V
		$V_{GS} = V_{DS}, I_D = -250 \mu\text{A}$	P	-1			
Gate-Body Leakage	I_{GS}	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$	P			± 100	nA
		$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	N			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	P			-1	μA
		$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$	N			1	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	N	20			A
		$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	P	-50			
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 33 \text{ A}$	N			36	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 28 \text{ A}$				46	
		$V_{GS} = -10 \text{ V}, I_D = -33 \text{ A}$	P			38	
		$V_{GS} = -4.5 \text{ V}, I_D = -28 \text{ A}$				48	
Forward Tranconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 33 \text{ A}$	N		40		S
		$V_{DS} = -15 \text{ V}, I_D = -33 \text{ A}$	P		31		
Dynamic							
Total Gate Charge	Q_g	N-Channel $V_{DS}=15\text{V}, V_{GS}=4.5\text{V}, I_D=33\text{A}$ P-Channel $V_{DS}=15\text{V}, V_{GS}=-4.5\text{V}, I_D=-33\text{A}$	N		12		nC
Gate-Source Charge	Q_{gs}		P		13		
Gate-Drain Charge	Q_{gd}		N		3.3		
			P		5.8		
			N		4.5		
			P		12		
Switching							
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel $V_{DD}=15\text{V}, V_{GS}=10\text{V}, I_D=1\text{A}$, $R_{GEN}=25\Omega$ P-Channel $V_{DD}=15\text{V}, V_{GS}=-10\text{V}, I_D=-1\text{A}$ $R_{GEN}=15\Omega$	N		20		nS
Rise Time	t_r		P		15		
Turn-Off Delay Time	$t_{d(off)}$		N		9		
Fall-Time	t_f		P		16		
			N		70		
			P		62		
			N		20		
			P		46		

Notes

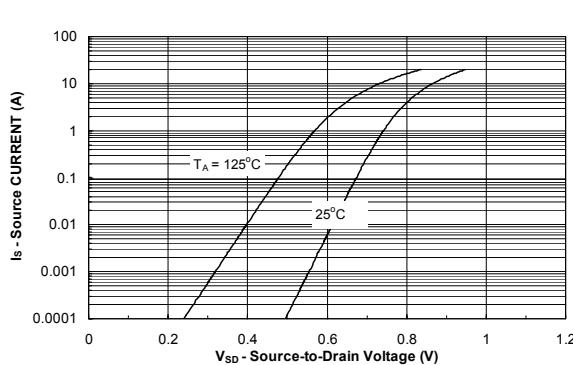
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

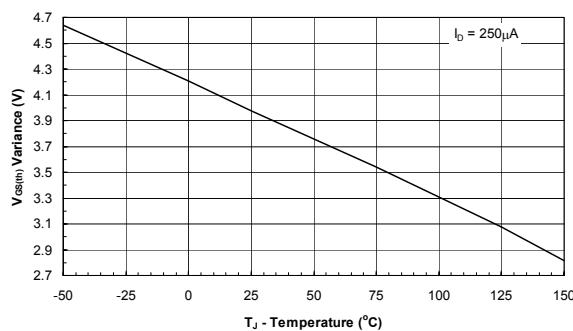
Typical Electrical Characteristics (N-Channel)



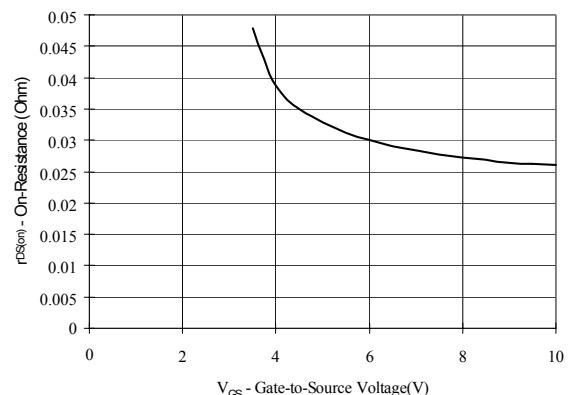
Typical Electrical Characteristics (N-Channel)



Source-Drain Diode Forward Voltage



Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

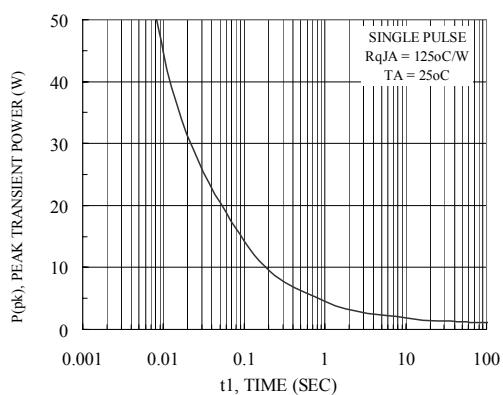


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

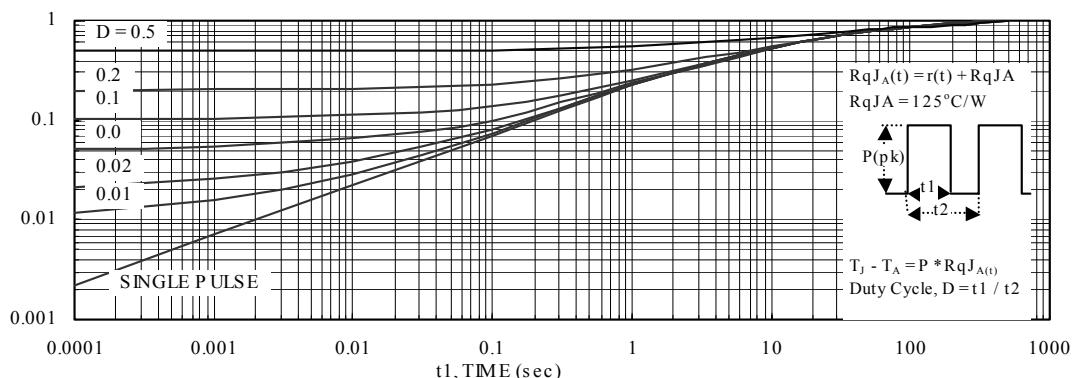
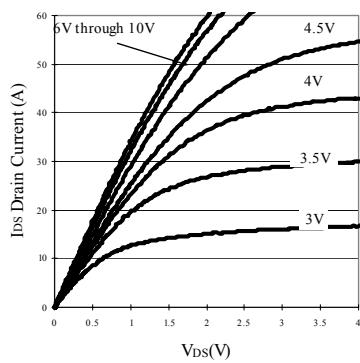
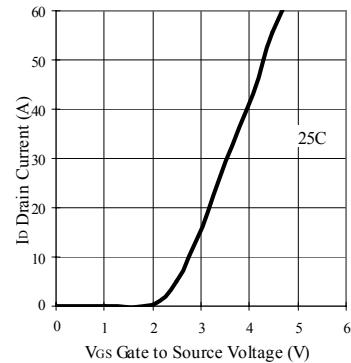


Figure 11. Transient Thermal Response Curve

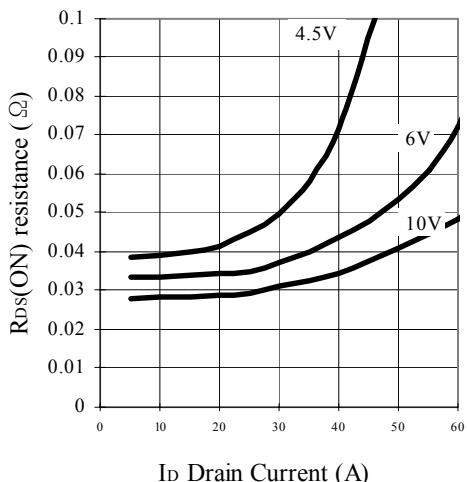
Typical Electrical Characteristics (P-Channel)



Output Characteristics

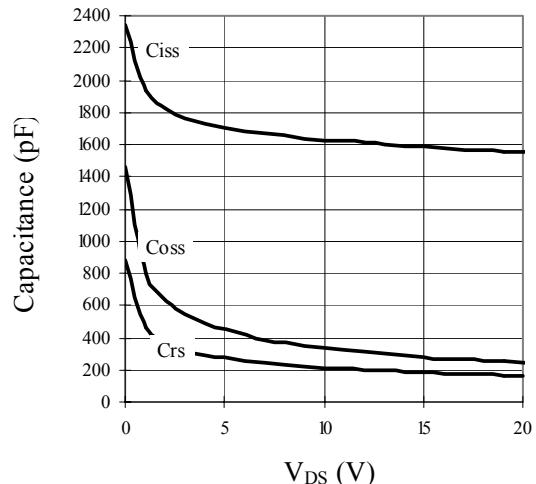


Transfer Characteristics

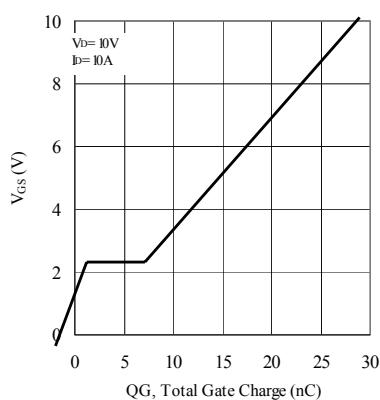


ID Drain Current (A)

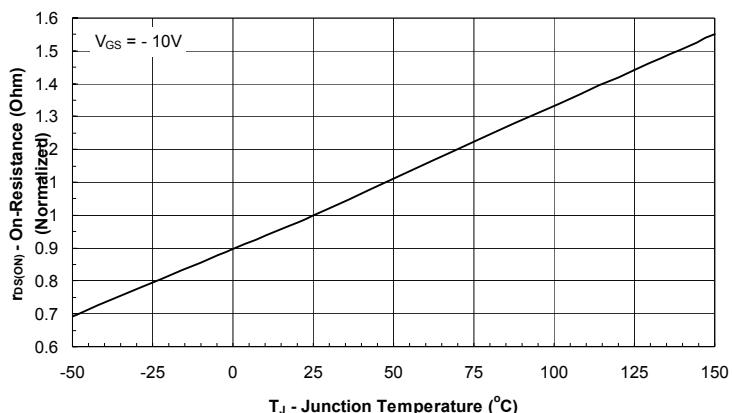
On Resistance Vs Vgs Voltage

 V_{DS} (V)

Capacitance

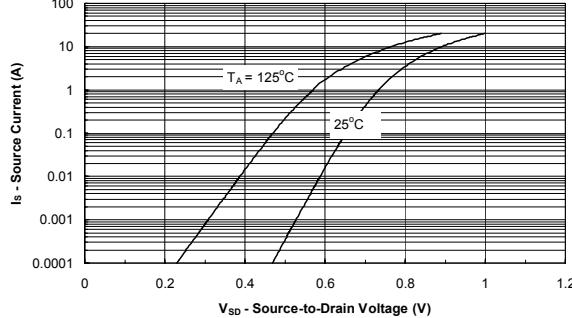


Gate Charge

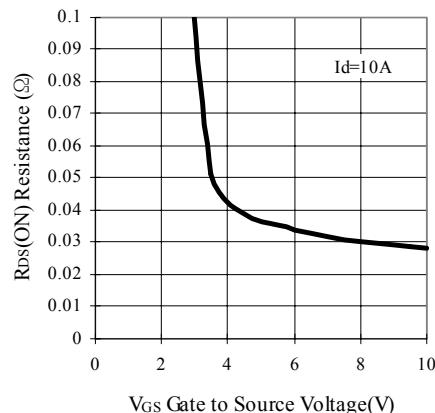


On-Resistance vs. Junction Temperature

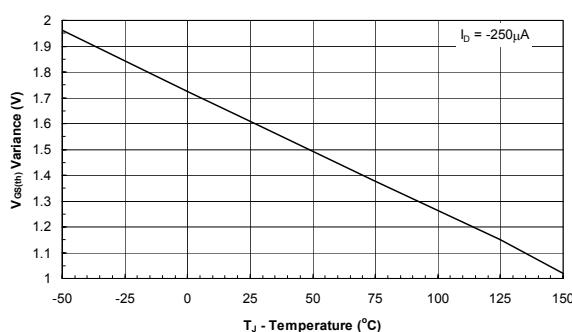
Typical Electrical Characteristics (P-Channel)



Source-Drain Diode Forward Voltage



On-Resistance with Gate to Source Voltage



Threshold Voltage

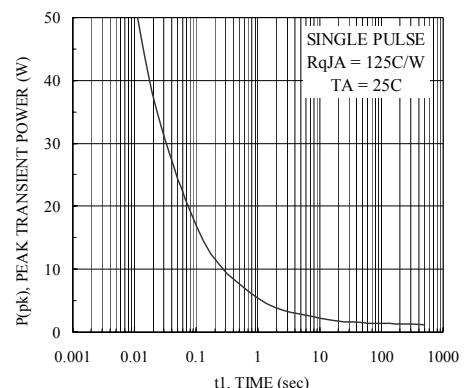


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

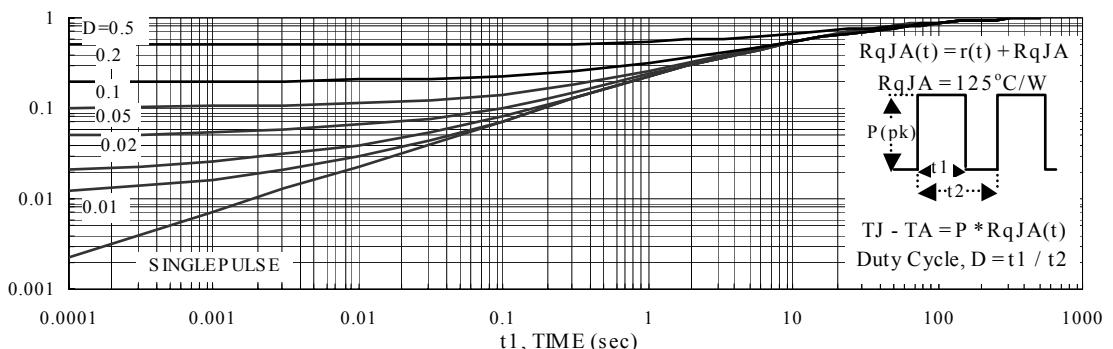
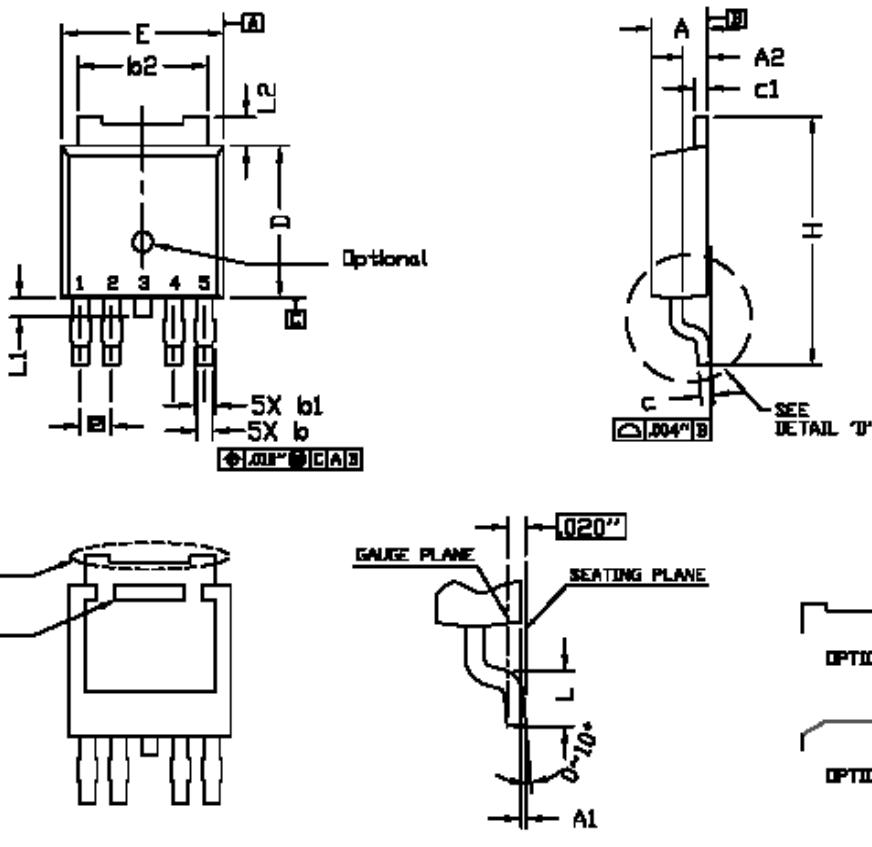


Figure 11. Transient Thermal Response Curve

TO252_4L PACKAGE OUTLINE



NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. DIMENSION L IS MEASURED IN GAUGE PLANE.
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED.
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AD).

SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.288	2.388	0.086	0.090	0.094
A1	0.000	—	0.127	0.000	—	0.005
A2	0.889	—	1.143	0.035	—	0.045
b	0.508	—	0.711	0.020	—	0.028
b1	0.584	—	0.787	0.023	—	0.031
b2	4.953	—	5.461	0.195	—	0.215
c	0.457	0.508	0.610	0.018	0.020	0.024
c1	0.457	—	0.610	0.018	—	0.024
D	5.989	6.096	6.223	0.235	0.240	0.245
E	6.350	6.804	6.731	0.250	0.260	0.265
e	1.270 BSC.			0.060 BSC.		
H	9.398	—	10.414	0.370	—	0.410
L	1.270	—	2.032	0.050	—	0.080
L1	—	—	1.016	—	—	0.040
L2	0.889	—	1.270	0.035	—	0.050