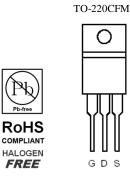
## N-Channel 100-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers.

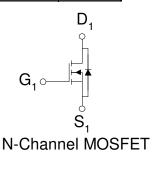
•	Low r <sub>DS(on)</sub> provides higher efficiency and
	extends battery life

- Low thermal impedance copper leadframe TO-220CFM saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$V_{DS}(V) \qquad r_{DS(on)} m(\Omega)$			
100	$16 @ V_{GS} = 10V$	87 <sup>a</sup>		
100	19 @ $V_{GS} = 5.5V$	87		



Top View



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		$V_{DS}$	100	V	
Gate-Source Voltage			±20	·	
Continuous Drain Current <sup>a</sup>	$T_C=25^{\circ}C$	$I_D$	87	_	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	240	A	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	90	A	
Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	$P_{\mathrm{D}}$	300	W	
Operating Junction and Storage Temperature Range		Tı, Tsto	-55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximm	Units		
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62.5	°C/W		
Maximum Junction-to-Case	$R_{ heta JC}$	3.2	°C/W		

1

## Notes

- a. Package Limited
- b. Pulse width limited by maximum junction temperature

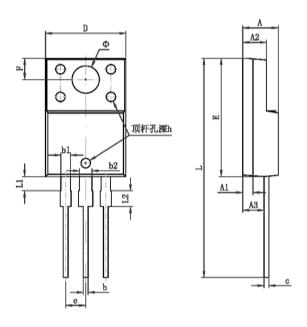
D (	G , ,	T . G . W.	Limits			<b>TT</b> •.	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250  uA$	1			V	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zero Gate Voltage Dialii Curient	IDSS	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			25	1 uA	
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			A	
D : G . C . D : . A	_	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$			16	mΩ	
Drain-Source On-Resistance <sup>A</sup>	r <sub>DS(on)</sub>	$V_{GS} = 5.5 \text{ V}, I_D = 2 \text{ A}$			19		
Forward Tranconductance <sup>A</sup>	$g_{\mathrm{fs}}$	$V_{DS} = 15 \text{ V}, I_D = 2 \text{ A}$		30		S	
Diode Forward Voltage	$V_{\mathrm{SD}}$	$I_S = 2 A$ , $V_{GS} = 0 V$		1.1		V	
Dynamic <sup>b</sup>	•		•		-	•	
Total Gate Charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 5.5 \text{ V},$		60			
Gate-Source Charge	$Q_{gs}$	$v_{DS} = 15 \text{ v}, v_{GS} = 5.5 \text{ v},$ $I_{D} = 2 \text{ A}$		19		nC	
Gate-Drain Charge	$Q_{gd}$	$I_D = 2 A$		39			
Turn-On Delay Time	t <sub>d(on)</sub>			25			
Rise Time	t <sub>r</sub>	$V_{\rm DD}$ = 25 V, $R_L$ = 25 $\Omega$ , Id = 2 A,		49		nS	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}$		111		113	
Fall-Time	$t_{\mathrm{f}}$			44			

## Notes

- a. Pulse test:  $PW \le 300$ us duty cycle  $\le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

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## Package Information



Symbol	Dimensions	In Millimeters	Dimension	s In Inches	
Symbol	Min	Max	Min	Max	
Α	4.300	4.700	0.169	0.185	
A1	1.300	1.300 REF		REF	
A2	2.800	3.200	0.110	0.126	
A3	2.500	2.900	0.098	0.114	
b	0.500	0.750	0.020	0.030	
b1	1.100	1.350	0.043	0.053	
b2	1.500	1.750	0.059	0.069	
С	0.500	0.750	0.020	0.030	
D	9.960	10.360	0.392	0.408	
E	14.800	15.200	0.583	0.598	
е	2.540	TYP	0.100 TYP		
F	2.700	REF	0.106	REF	
Ф	3.500	REF	0.138	REF	
h	0.000	0.300	0.000	0.012	
L	28.000	28.400	1.102	1.118	
L1	1.700	1.900	0.067	0.075	
L2	1.900	2.100	0.075	0.083	