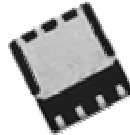


P-Channel 80-V (D-S) MOSFET

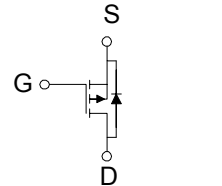
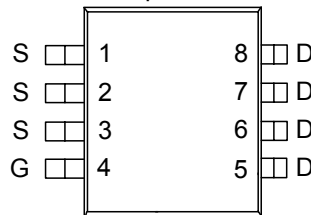
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-80	75 @ $V_{GS} = -10V$	-6.7
	90 @ $V_{GS} = -4.5V$	-6.1

SOIC-8PP
Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-6.7	A
	$T_A = 70^\circ\text{C}$		-5.0	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.1	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.0	W
	$T_A = 70^\circ\text{C}$		3.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	25	$^\circ\text{C/W}$
	Steady State		65	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

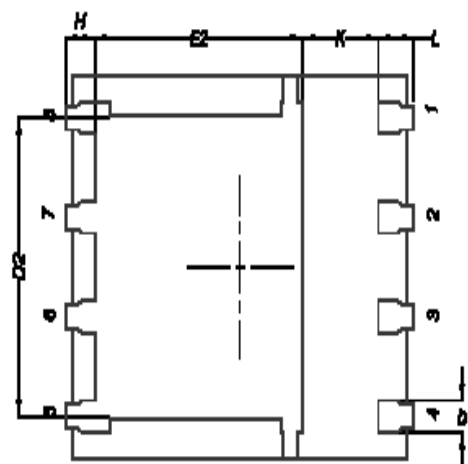
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-30			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -64\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -64\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -10\text{ V}$	-50			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = -10\text{ V}$, $I_D = -6.7\text{ A}$			75	m Ω
		$V_{GS} = -4.5\text{ V}$, $I_D = -6.1\text{ A}$			90	
Forward Transconductance ^A	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -6.7\text{ A}$		29		S
Diode Forward Voltage	V_{SD}	$I_S = 2.5\text{ A}$, $V_{GS} = 0\text{ V}$		-0.8		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}$, $V_{GS} = -5\text{ V}$, $I_D = -6.7\text{ A}$		25		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			17		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}$, $R_L = 6\text{ }\Omega$, $I_D = -1\text{ A}$, $V_{GEN} = -10\text{ V}$		15		nS
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{d(off)}$			100		
Fall-Time	t_f			54		

Notes

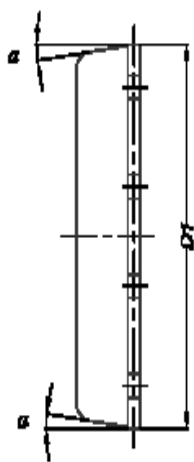
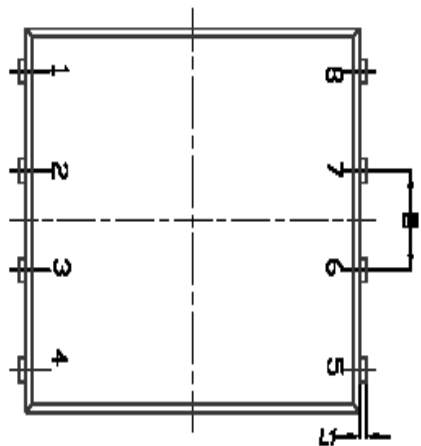
- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



BACKSIDE VIEW



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.90	4.90	5.00
D2	3.81	3.81	3.98
E	5.00	6.00	6.10
E1	5.70	6.75	6.80
E2	3.98	3.98	3.78
Ø	1.27 BSC		
H	0.41	0.51	0.51
K	1.10	-	-
L	0.51	0.51	0.71
L1	0.08	0.13	0.20
α	0°	-	12°

