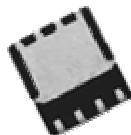


N-Channel 60-V (D-S) MOSFET

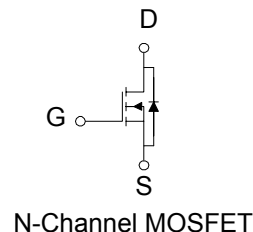
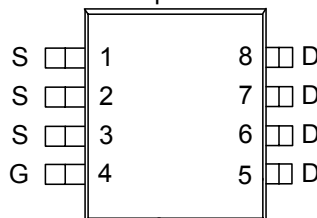
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
60	82 @ $V_{GS} = 10V$	6.4
	115 @ $V_{GS} = 4.5V$	5.4

SOIC-8PP
Top View



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	6.4	A
	$T_A = 70^\circ\text{C}$		5.3	
Pulsed Drain Current ^b		I_{DM}	20	
Continuous Source Current (Diode Conduction) ^a		I_S	2.3	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.0	W
	$T_A = 70^\circ\text{C}$		3.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	25	$^\circ\text{C/W}$
	Steady State		65	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

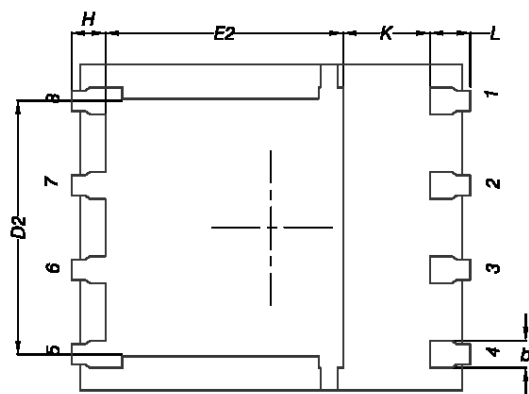
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 12 V			100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48 V, V _{GS} = 0 V			1	uA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 55°C			5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	40			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 2 A			82	mΩ
		V _{GS} = 4.5 V, I _D = 2 A			115	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 6 A		40		S
Diode Forward Voltage	V _{SD}	I _S = 2.3 A, V _{GS} = 0 V		0.7		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 6 A		15		nC
Gate-Source Charge	Q _{gs}			3		
Gate-Drain Charge	Q _{gd}			5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 6 Ω , I _D = 1 A, V _{GEN} = 10 V		15		nS
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(off)}			54		
Fall-Time	t _f			26		

Notes

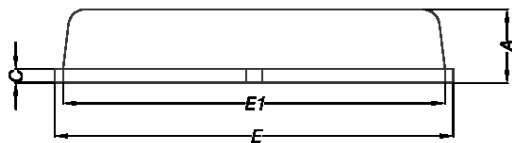
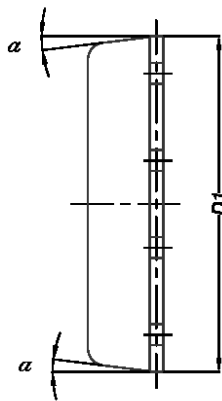
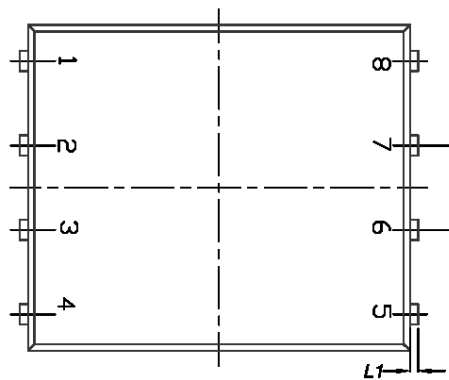
- Pulse test: $PW \leq 300\text{ }\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



BACKSIDE VIEW



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
Ø	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°