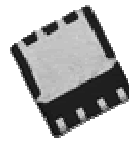


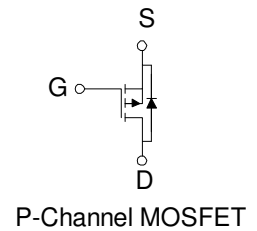
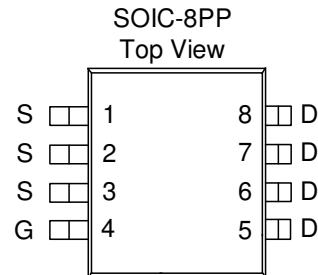
P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-20	5 @ $V_{GS} = -4.5V$	-26
	7 @ $V_{GS} = -2.5V$	-22



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-26	A
	$T_A = 70^\circ\text{C}$		-22	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.1	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.0	W
	$T_A = 70^\circ\text{C}$		3.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	25	$^\circ\text{C/W}$
	Steady State		65	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

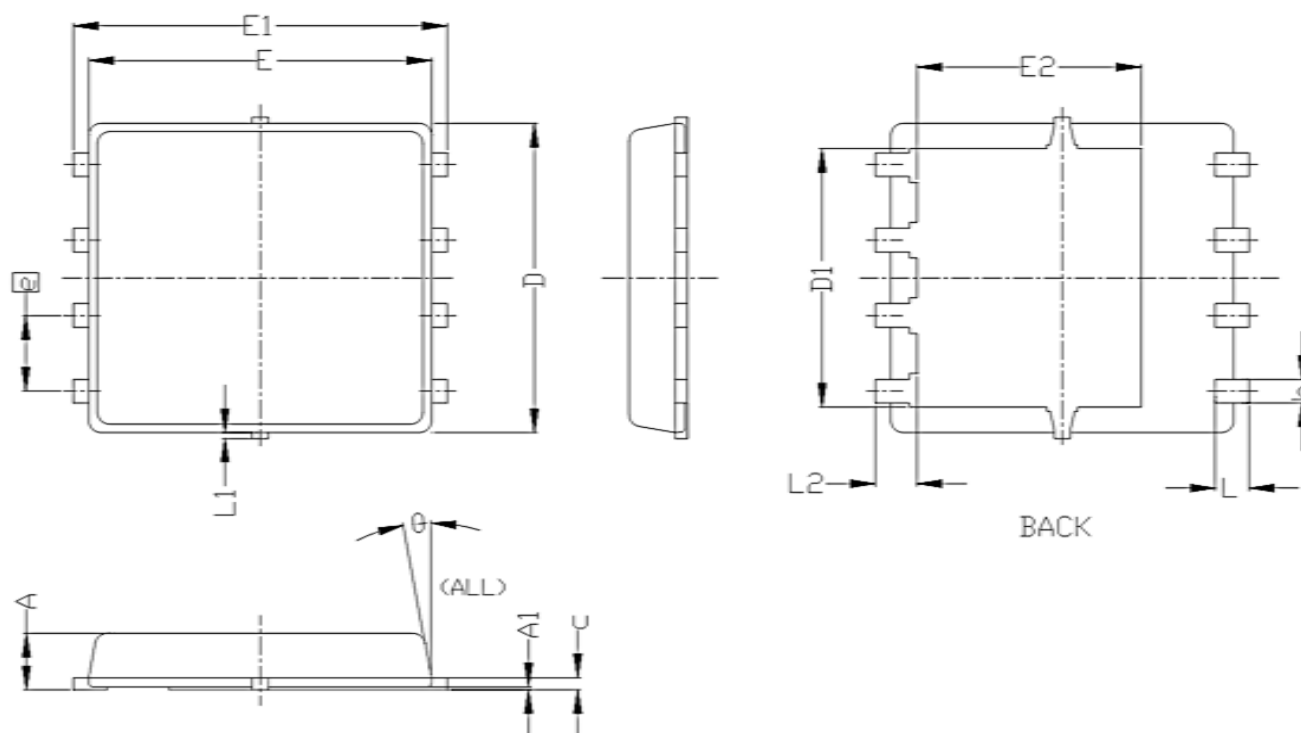
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.4			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -4.5 V, V _{GS} = -10 V	-50			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -1 A			5	mΩ
		V _{GS} = -2.5 V, I _D = -1 A			7	
Forward Tranconductance ^A	g _{fs}	V _{DS} = -15 V, I _D = -1 A		70		S
Diode Forward Voltage	V _{SD}	I _S = 1 A, V _{GS} = 0 V		-0.6		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -1 A		200		nC
Gate-Source Charge	Q _{gs}			20		
Gate-Drain Charge	Q _{gd}			70		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 6 Ω , I _D = -1 A, V _{GEN} = -4.5 V		40		nS
Rise Time	t _r			100		
Turn-Off Delay Time	t _{d(off)}			900		
Fall-Time	t _f			500		

Notes

- Pulse test: $PW \leq 300\text{us}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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Package Information



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.62 BSC			0.143 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°