

N-Channel 120-V (D-S) MOSFET

Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

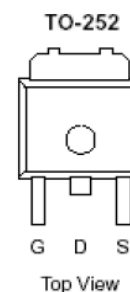
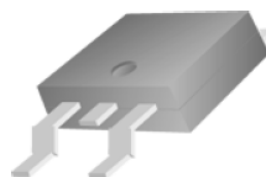
Typical Applications:

- LED Inverter Circuits
- DC/DC Conversion Circuits
- Motor drives

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
120	10 @ $V_{GS} = 10V$	52
	14 @ $V_{GS} = 6.5V$	44



RoHS
COMPLIANT
HALOGEN
FREE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	120	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	52	A
Pulsed Drain Current ^b		I_{DM}	200	
Continuous Source Current (Diode Conduction) ^a	$T_C = 25^\circ\text{C}$	I_S	52	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	40	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^c	$R_{\theta JA}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3	

Notes

- Package Limited
- Pulse width limited by maximum junction temperature
- Surface Mounted on 1" x 1" FR4 Board.

Electrical Characteristics

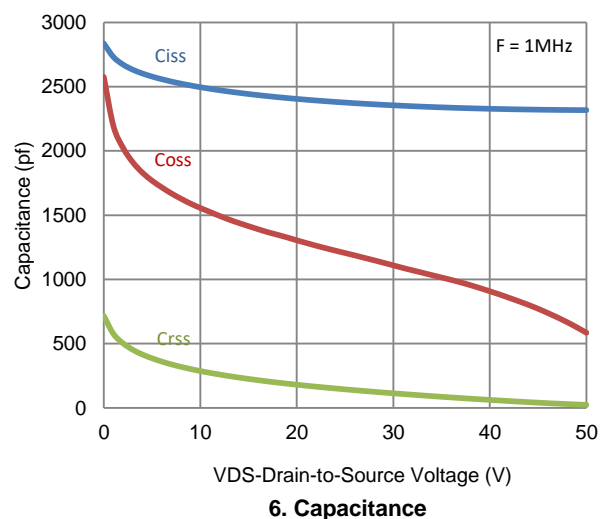
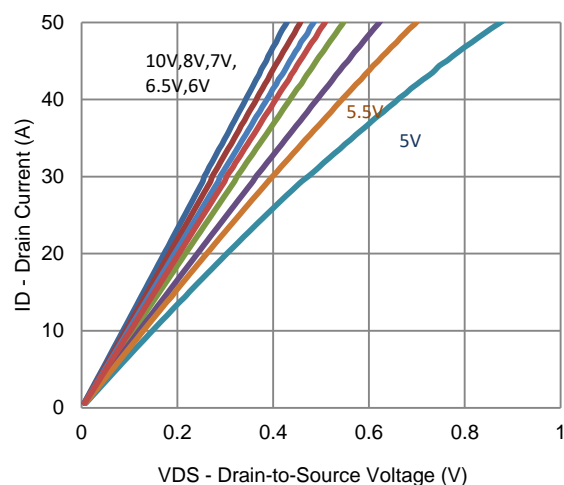
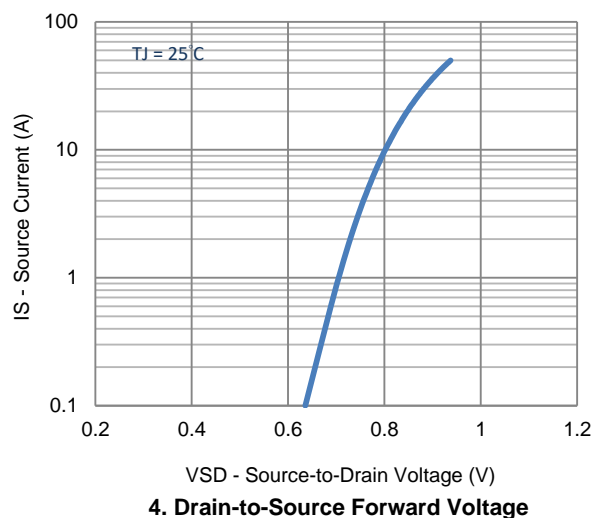
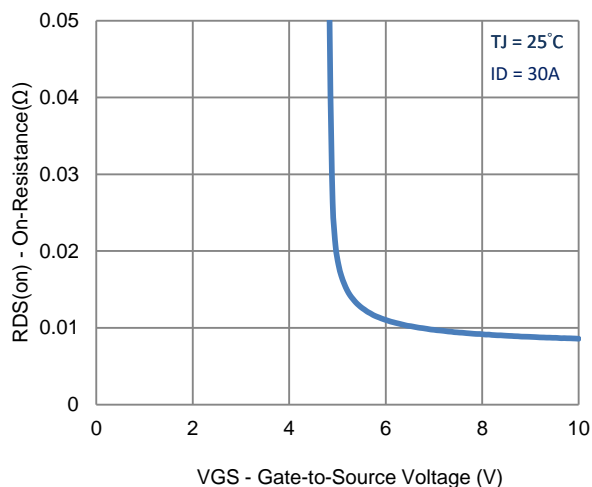
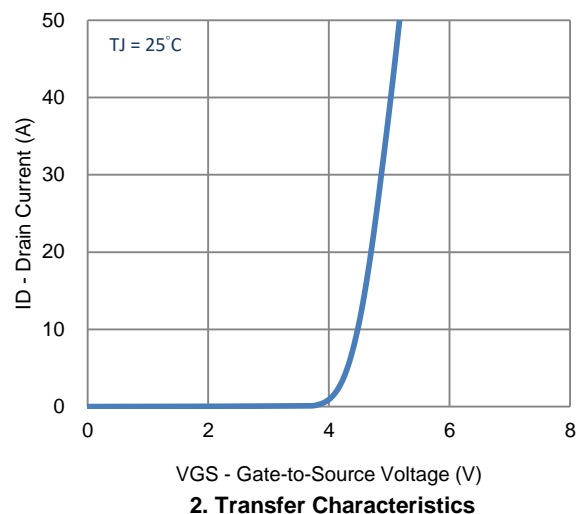
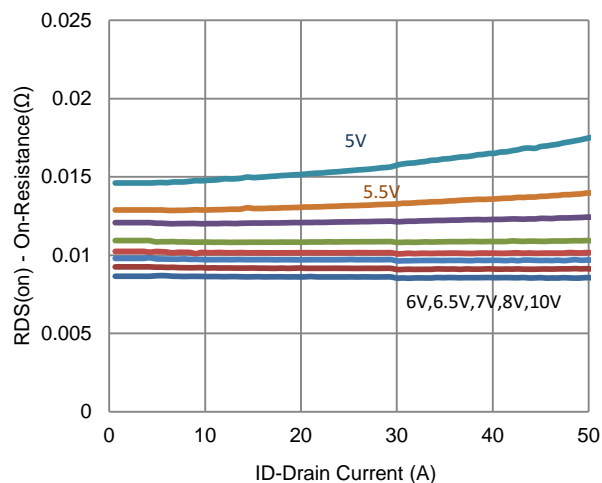
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 96 V$, $V_{GS} = 0 V$			1	μA
		$V_{DS} = 96 V$, $V_{GS} = 0 V$, $T_J = 55^\circ C$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 V$, $V_{GS} = 10 V$	90			A
Drain-Source On-Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 V$, $I_D = 30 A$			10	m Ω
		$V_{GS} = 6.5 V$, $I_D = 25 A$			14	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 V$, $I_D = 30 A$		58		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 30 A$, $V_{GS} = 0 V$		0.88		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 60 V$, $V_{GS} = 6.5 V$, $I_D = 30 A$		30		nC
Gate-Source Charge	Q_{gs}			12		
Gate-Drain Charge	Q_{gd}			12		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 60 V$, $R_L = 2 \Omega$, $I_D = 30 A$, $V_{GEN} = 10 V$, $R_{GEN} = 6 \Omega$		17		ns
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(off)}$			47		
Fall Time	t_f			68		
Input Capacitance	C_{iss}	$V_{DS} = 50 V$, $V_{GS} = 0 V$, $f = 1 Mhz$		2318		pF
Output Capacitance	C_{oss}			585		
Reverse Transfer Capacitance	C_{rss}			24		

Notes

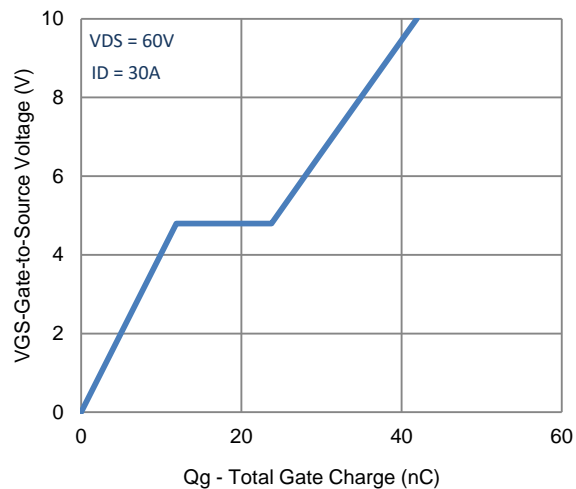
- Pulse test: PW \leq 300us duty cycle \leq 2%.
- Guaranteed by design, not subject to production testing.

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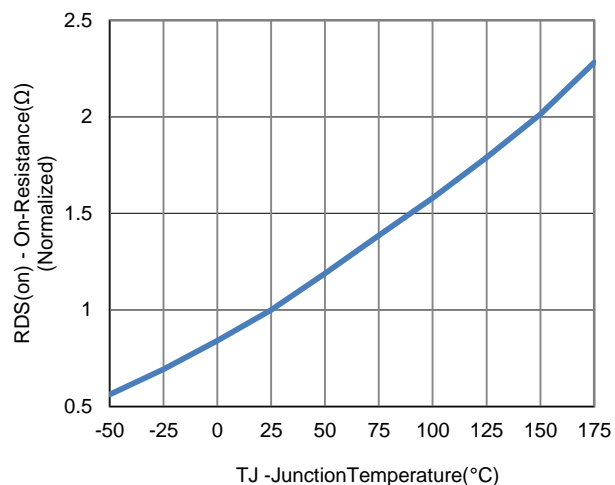
Typical Electrical Characteristics



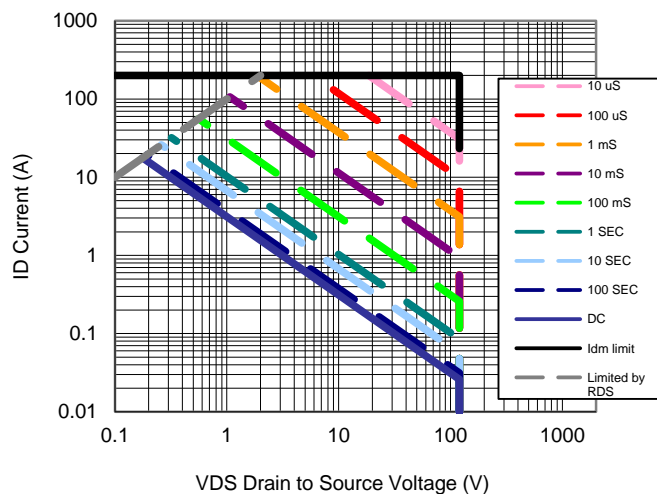
Typical Electrical Characteristics



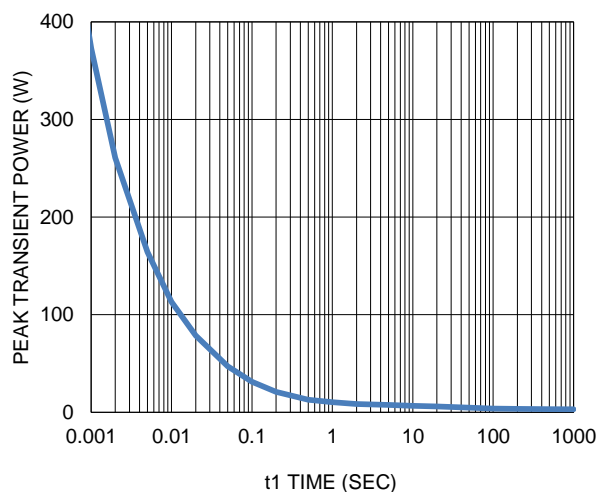
7. Gate Charge



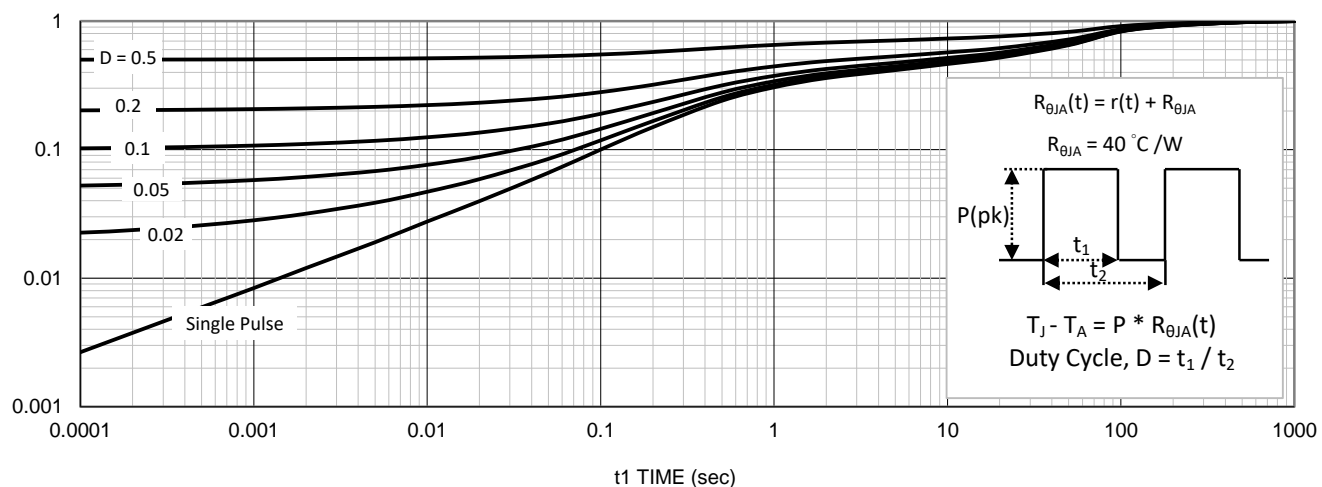
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

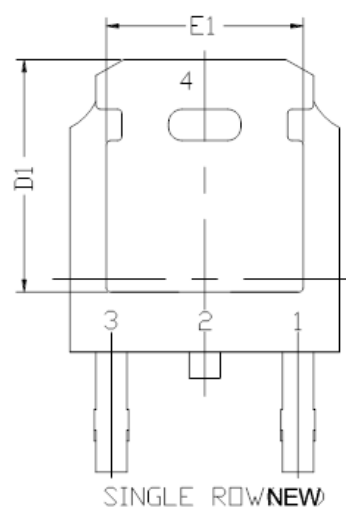
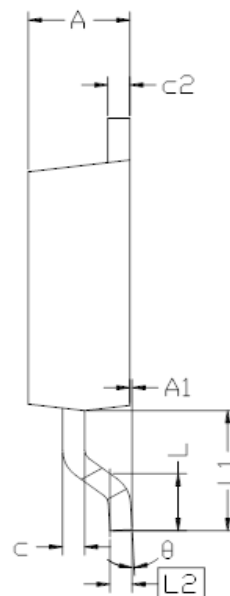
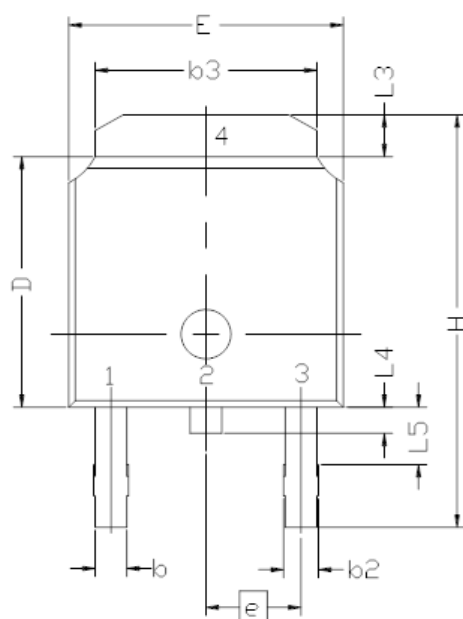


10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

Package Information



SINGLE ROW NEW

SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	--	--
E1	4.40	--	--
θ	0°	--	10°

Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.