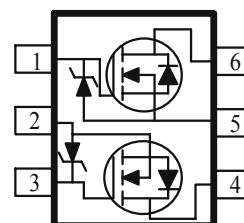
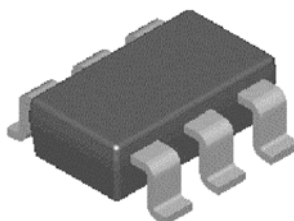


Dual N-Channel Logic Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low  $r_{DS(on)}$  and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low  $r_{DS(on)}$  provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (OHM)	$I_D$ (A)
25	4.0 @ $V_{GS} = 4.5$ V	0.4
	5.1 @ $V_{GS} = 2.5$ V	0.2



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	-8.5	
Continuous Drain Current <sup>a</sup>	$I_D$	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	0.5	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	$\pm 0.3$	A
Power Dissipation <sup>a</sup>	$P_D$	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{THJA}$	t $\leq$ 5 sec	$^\circ\text{C/W}$
		Steady-State	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
<b>Switch Off Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	0.67	0.85	1.5	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 8\text{ V}$			100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	uA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	
<b>Switch On Characteristics</b>						
On-State Drain Current <sup>A</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 2.5\text{ V}$	0.2			A
Drain-Source On-Resistance <sup>A</sup>	$r_{DS(on)}$	$V_{GS} = 2.5\text{ V}, I_D = 0.2\text{ A}$		3.8	5.0	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 0.2\text{ A}, T_J = 55^\circ\text{C}$		4.0	5.5	
		$V_{GS} = 4.5\text{ V}, I_D = 0.4\text{ A}$		3.1	4.0	
Forward Transconductance <sup>A</sup>	$g_{fs}$	$V_{DS} = 5\text{ V}, I_D = 0.4\text{ A}$		0.25		S
Diode Forward Voltage	$V_{SD}$	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		0.85	1.20	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.2\text{ A}$		0.5	0.71	nC
Gate-Source Charge	$Q_{gs}$			0.22		
Gate-Drain Charge	$Q_{gd}$			0.07		
Input Capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		10		pF
Output Capacitance	$C_{oss}$			6		
Reverse Transfer Capacitance	$C_{rss}$			2		
<b>Switching</b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\text{ V}, I_D = 0.5\text{ A},$ $V_{GEN} = 4.5\text{ V}, R_G = 50\text{ }\Omega$		5	10	ns
Rise Time	$t_r$			4.5	10	
Turn-Off Delay Time	$t_{d(off)}$			4	8	
Fall-Time	$t_f$			3.2	7	

## Notes

- Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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### Typical Electrical Characteristics

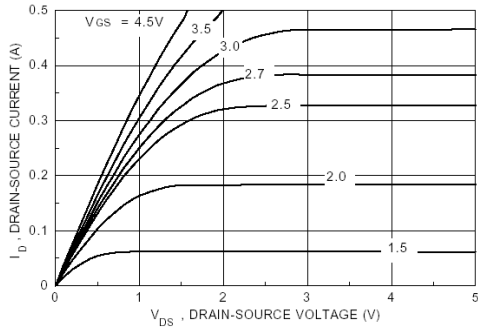


Figure 1. On-Region Characteristics

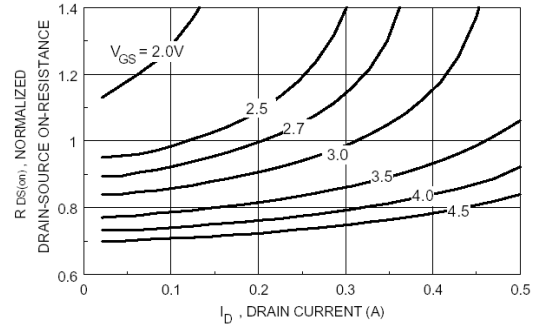


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

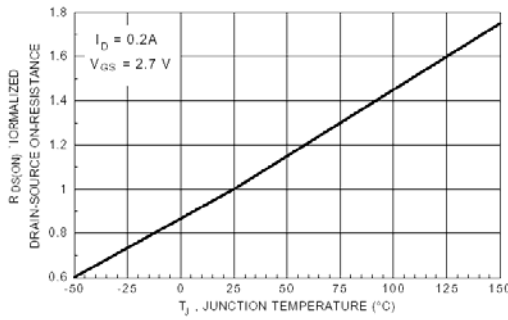


Figure 3. On-Resistance Variation with Temperature

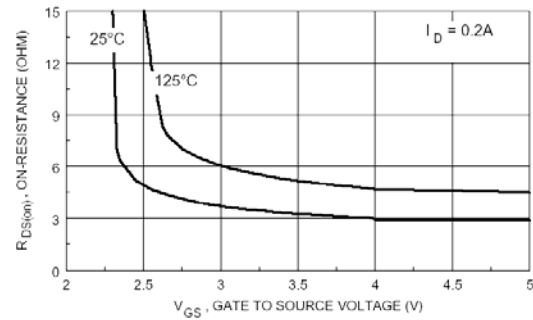


Figure 4. On-Resistance Variation with Gate to Source Voltage

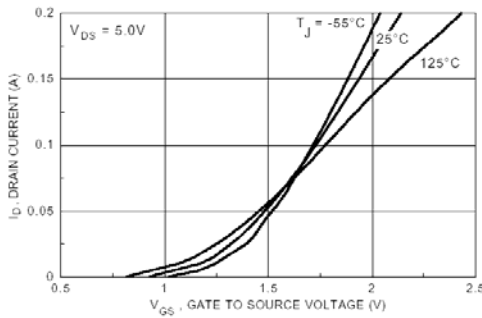


Figure 5. Transfer Characteristics

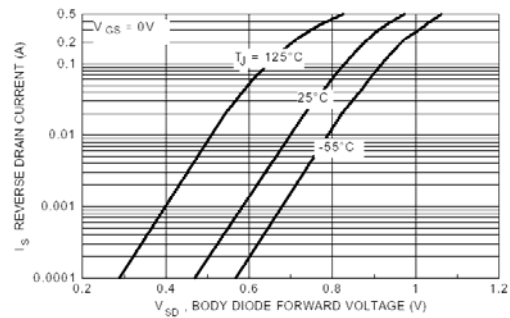


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

### Typical Electrical Characteristics

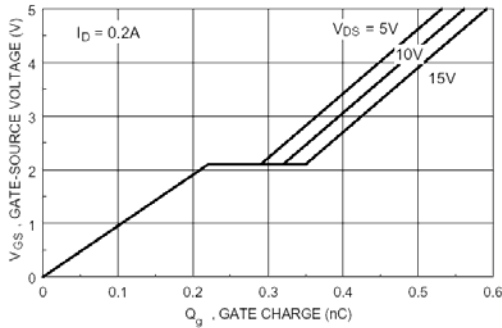


Figure 7. Gate Charge Characteristics

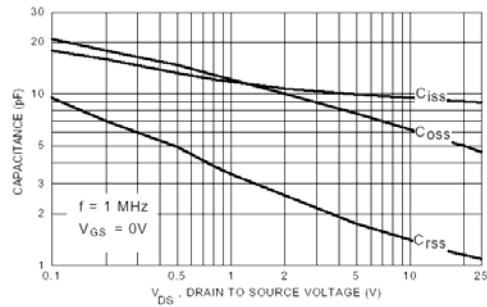


Figure 8. Capacitance Characteristics

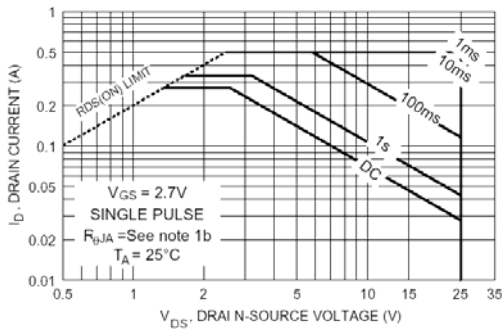


Figure 9. Maximum Safe Operating Area

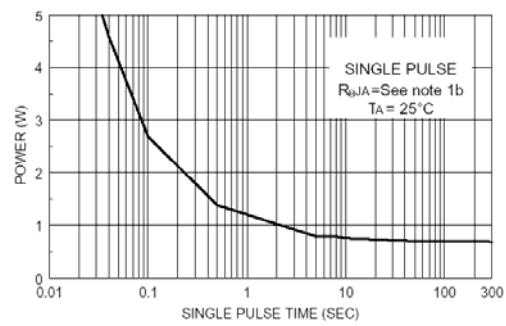


Figure 10. Single Pulse Maximum Power Dissipation

### Normalized Thermal Transient Junction to Ambient

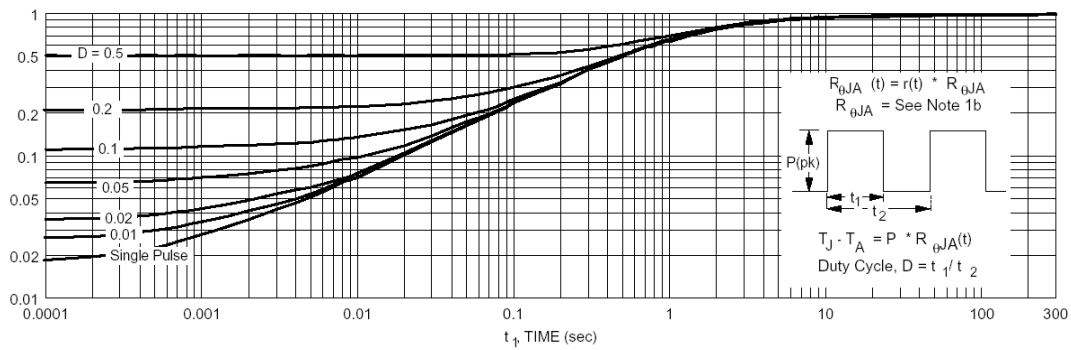
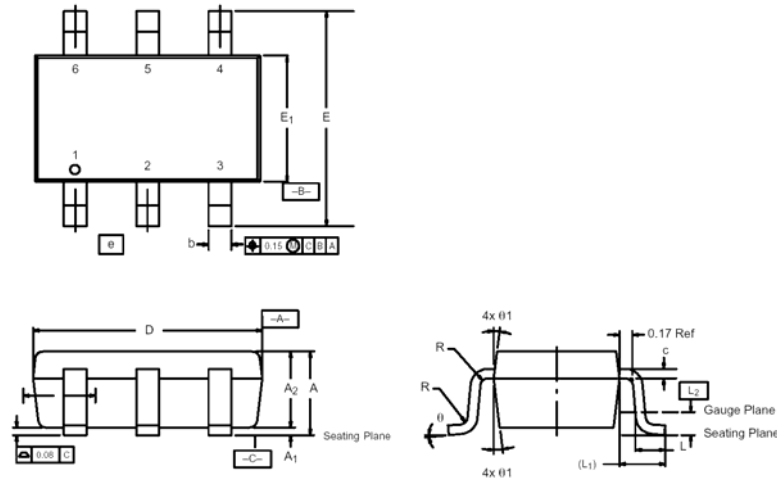


Figure 11. Transient Thermal Response Curve

Package Information

TSOP-6: 6LEAD



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	—	1.10	0.036	—	0.043
A <sub>1</sub>	0.01	—	0.10	0.0004	—	0.004
A <sub>2</sub>	0.84	—	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
L	0.35	—	0.50	0.014	—	0.020
L <sub>1</sub>	0.60 Ref			0.024 Ref		
L <sub>2</sub>	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
Ø	0°	4°	8°	0°	4°	8°
Ø <sub>1</sub>	7° Nom			7° Nom		