# N-Channel 150-V (D-S) MOSFET

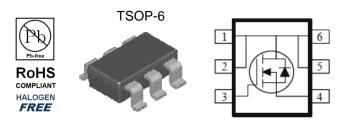
### **Key Features:**

- Low r<sub>DS(on)</sub> trench technology
- · Low thermal impedance
- · Fast switching speed

## **Typical Applications:**

- PoE PSE and PD Circuits
- LED Inverter Circuits
- 48V-Input DC/DC Conversion Circuits

PRODUCT SUMMARY			
Vds (V)	$r_{DS(on)}(m\Omega)$	I⊳(A)	
150	245 @ V <sub>GS</sub> = 10V	2.4	
150	288 @ V <sub>GS</sub> = 6.5V	2.2	



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}C$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V <sub>DS</sub>	150	V	
Gate-Source Voltage			±20	V	
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25°C	I	2.4	А	
Continuous Drain Current	T <sub>A</sub> =70°C	I <sub>D</sub>	1.9		
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	10			
Continuous Source Current (Diode Conduction) <sup>a</sup>		ا <sub>s</sub>	3.1	А	
Device Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	P <sub>D</sub>	2	W	
Power Dissipation <sup>a</sup>	T <sub>A</sub> =70°C	гD	1.3	vv	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient <sup>a</sup>	t <= 10 sec	$R_{\thetaJA}$	62.5	°C/W	
	Steady State	ιν <sub>θ</sub> ja	110		

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

# **Electrical Characteristics**

Parameter	Symbol	Test Conditions	Min	Тур	Мах	Unit	
Static							
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA	
Zero Gate Voltage Drain Current	1	$V_{DS} = 120 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	uA	
	DSS	$V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 V, V_{GS} = 10 V$	3.5			А	
	r	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 2 \text{ A}$			245	mΩ	
Drain-Source On-Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 6.5 \text{ V}, \text{ I}_{D} = 1.6 \text{ A}$			288		
Forward Transconductance <sup>a</sup>	<b>g</b> <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 2 \text{ A}$		6		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{S} = 1.3 \text{ A}, V_{GS} = 0 \text{ V}$		0.71		V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 6.5 V,		3.7			
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 73$ V, $V_{GS} = 0.3$ V, $I_{D} = 2$ A		0.8		nC	
Gate-Drain Charge	Q <sub>gd</sub>	$I_D = Z \Lambda$		1.9			
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 75 V, R <sub>L</sub> = 37.5 Ω,		2			
Rise Time	t <sub>r</sub>	$V_{DS} = 75 V$ , $R_L = 57.5 \Omega_2$ , $I_D = 2 A$ .		3		20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{GEN}} = 6 \Omega$		8		ns	
Fall Time	t <sub>f</sub>	V GEN - 10 V, INGEN - 0 12		4			
Input Capacitance	C <sub>iss</sub>			242			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		35		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			43			

#### Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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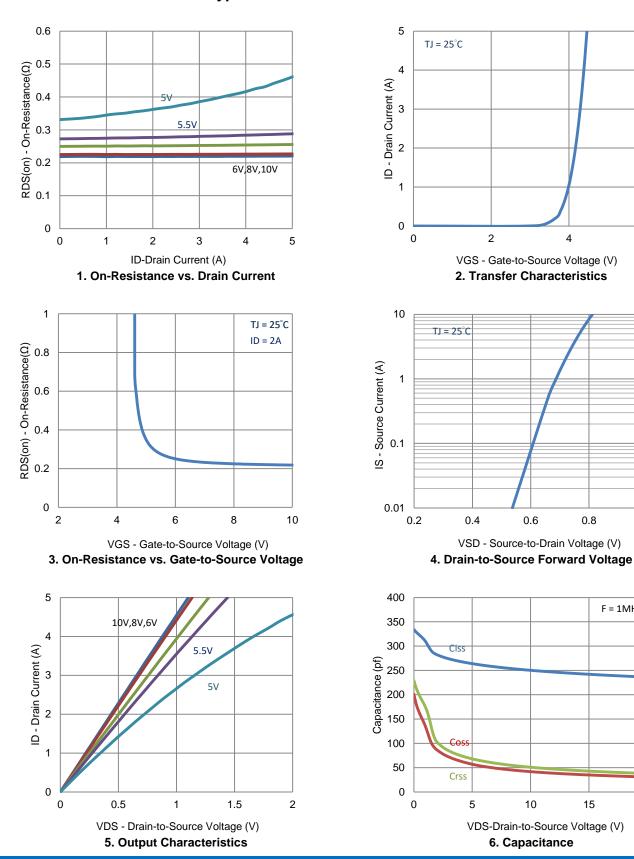
1

20

F = 1MHz

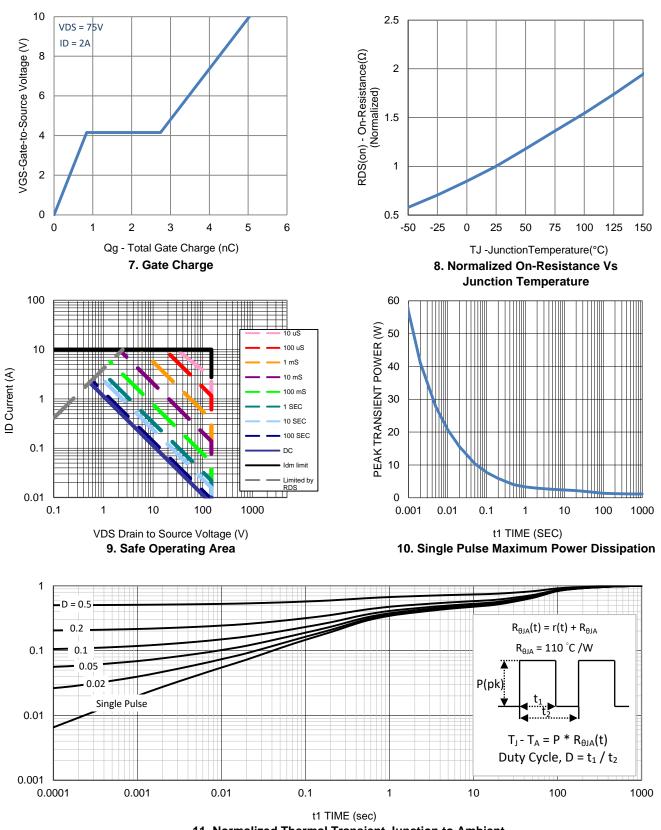
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0.8



# **Typical Electrical Characteristics**

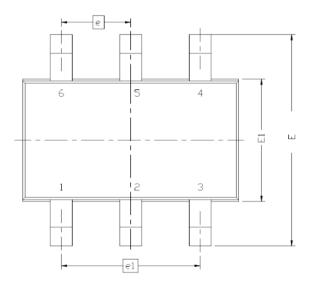
15



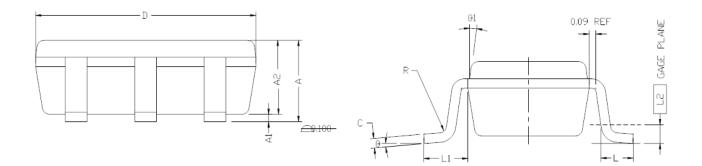
# **Typical Electrical Characteristics**

11. Normalized Thermal Transient Junction to Ambient

# **Package Information**



DIM.	MILLIMETERS				
DIM.	MIN	NDM	MAX		
Α	0.935		1.10		
A1	0.01		0.10		
A2	0.70		1.00		
b	0.25	0.32	0.40		
$\subset$	0.10	0.15	0.20		
D	2.95	3.05	3.10		
Ε	2.70	2.85	2.98		
E1	1.55	1.65	1.70		
e	0.95 BSC				
L	0.30		0.60		
L1	0.60REF				
L2	0.25BSC				
R	0.10				
θ	0?	4?	8?		
θ1	7? NDM				



Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
- 4. The Package Top May Be Smaller Than The Package Bottom.
- 5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.