

## N-Channel 100-V (D-S) MOSFET

### Key Features:

- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed

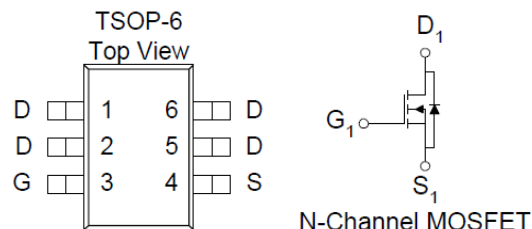
### Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
100	280 @ $V_{GS} = 10V$	2.2
	355 @ $V_{GS} = 4.5V$	2.0



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	2.2	A
	$T_A = 70^\circ\text{C}$		1.8	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	10	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	2.5	A
Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
	Steady State		110	

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

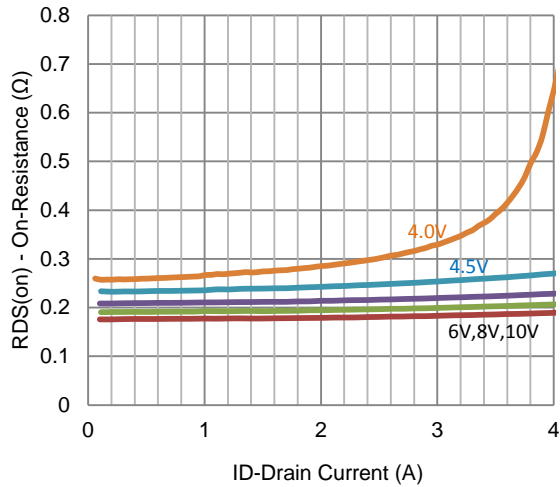
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		3.5	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80 V, V_{GS} = 0 V$			1	uA
		$V_{DS} = 80 V, V_{GS} = 0 V, T_J = 55^\circ C$			25	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	5			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 1.5 A$			280	m $\Omega$
		$V_{GS} = 4.5 V, I_D = 1.4 A$			355	
Forward Transconductance	$g_{fs}$	$V_{DS} = 15 V, I_D = 1.5 A$		5		S
Diode Forward Voltage	$V_{SD}$	$I_S = 1.3 A, V_{GS} = 0 V$		0.77		V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 1.5 A$		4.1		nC
Gate-Source Charge	$Q_{gs}$			1.4		
Gate-Drain Charge	$Q_{gd}$			1.9		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50 V, R_L = 33.3 \Omega, I_D = 1.5 A,$ $V_{GEN} = 10 V, R_{GEN} = 6 \Omega$		5.7		ns
Rise Time	$t_r$			4.3		
Turn-Off Delay Time	$t_{d(off)}$			12.8		
Fall-Time	$t_f$			4.4		
Input Capacitance	$C_{iss}$	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz$		332		pF
Output Capacitance	$C_{oss}$			40		
Reverse Transfer Capacitance	$C_{rss}$			29		

## Notes

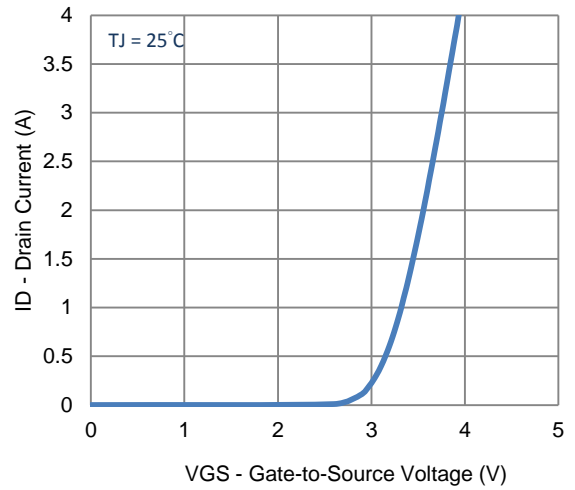
- Pulse test: PW  $\leq$  300us duty cycle  $\leq$  2%.
- Guaranteed by design, not subject to production testing.

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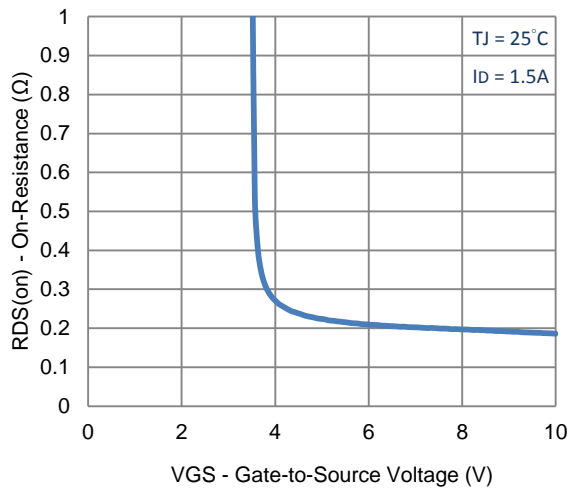
Typical Electrical Characteristics



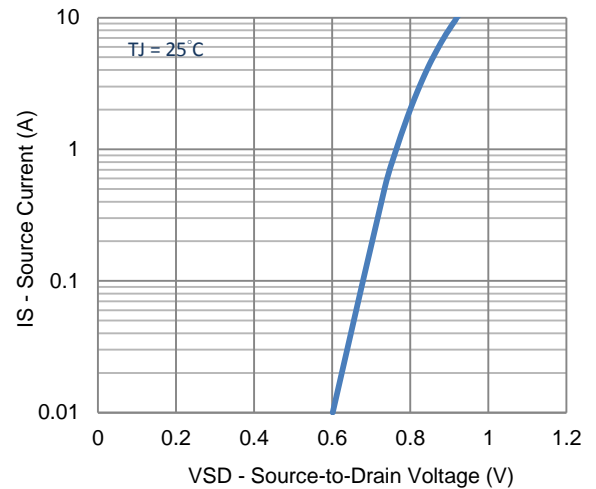
1. On-Resistance vs. Drain Current



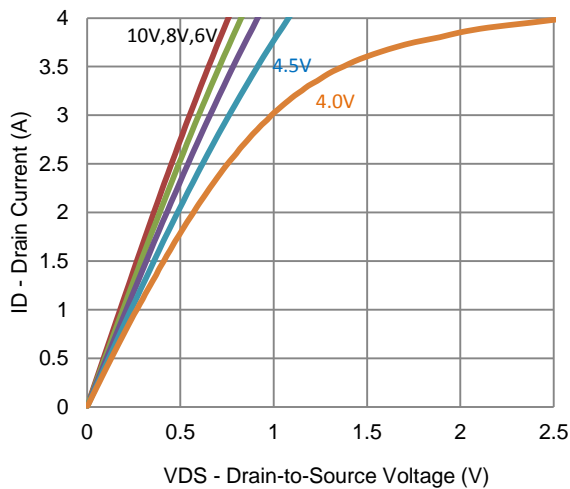
2. Transfer Characteristics



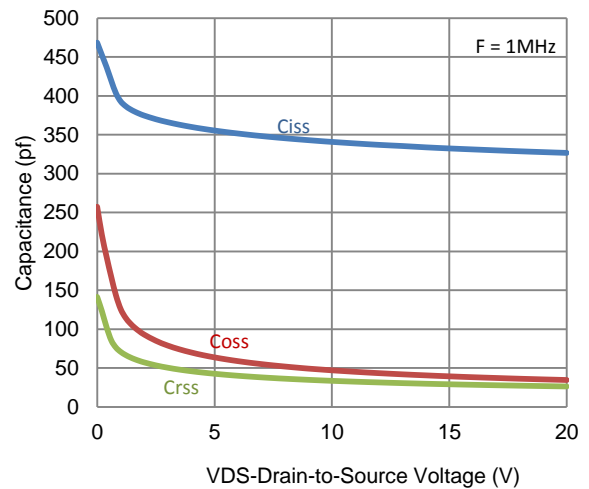
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

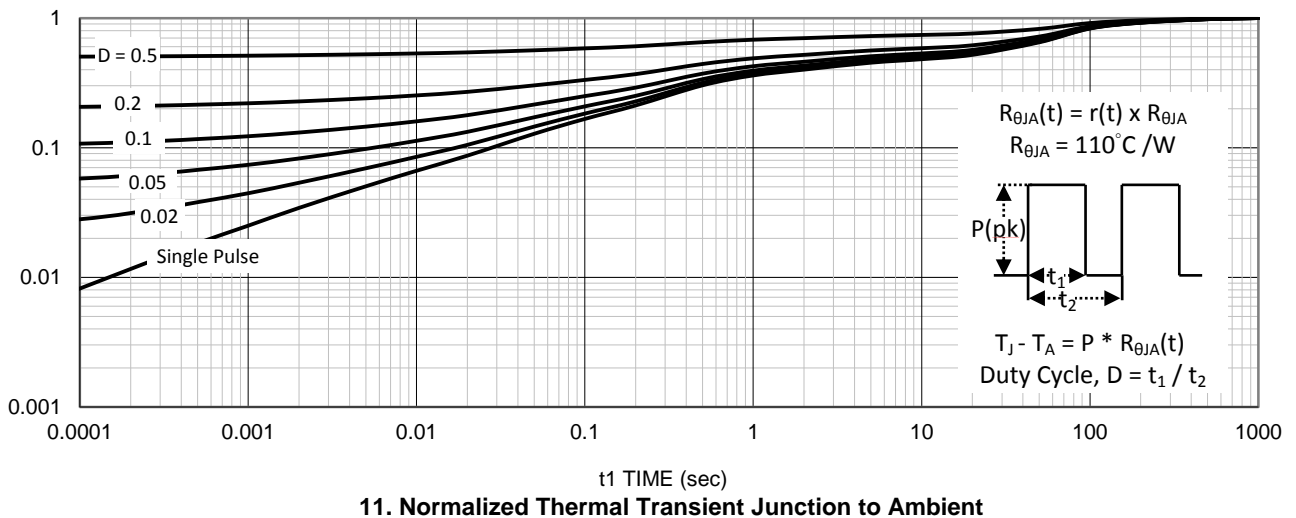
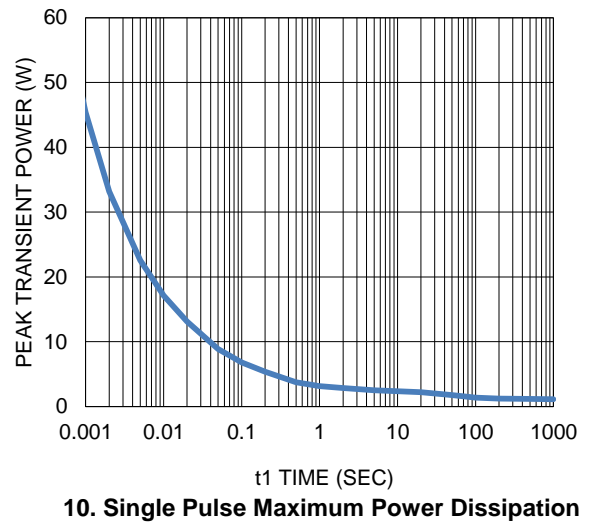
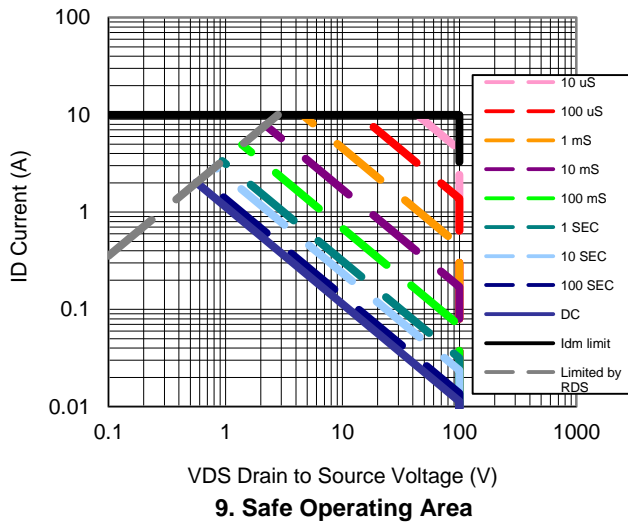
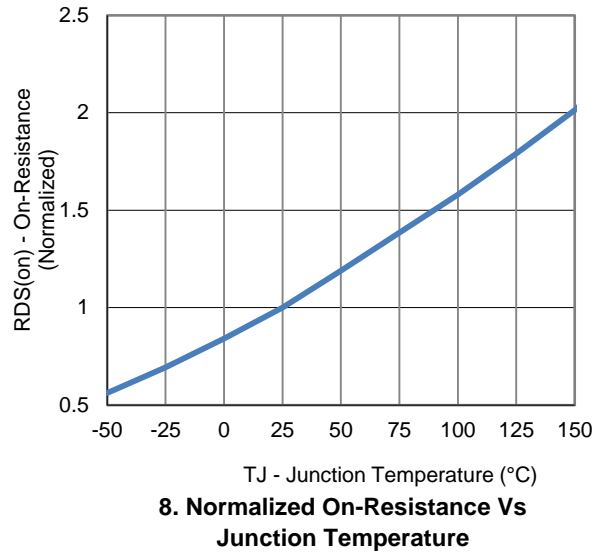
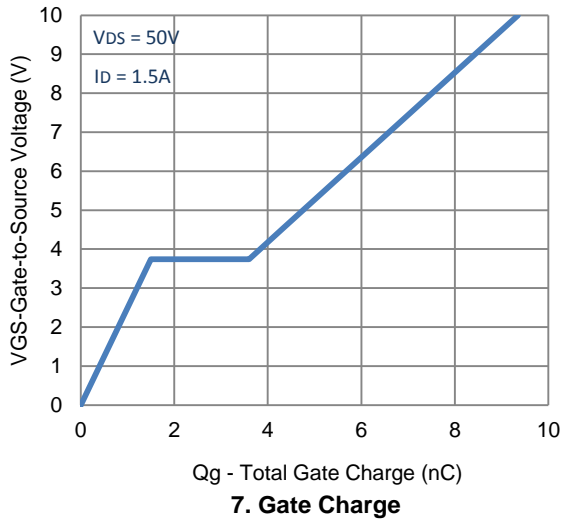


5. Output Characteristics

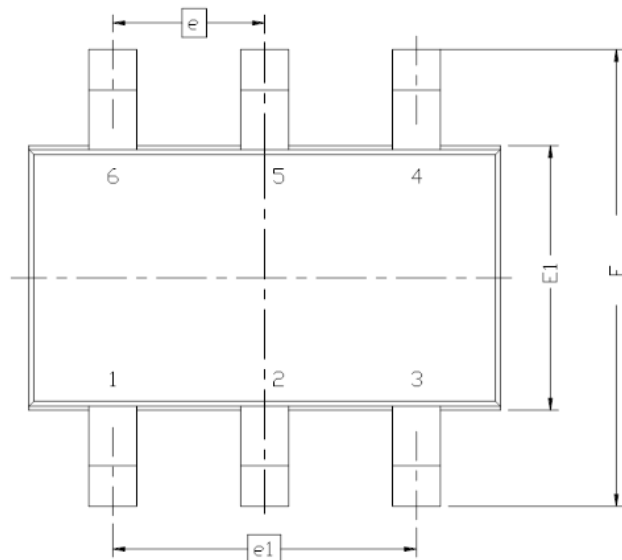


6. Capacitance

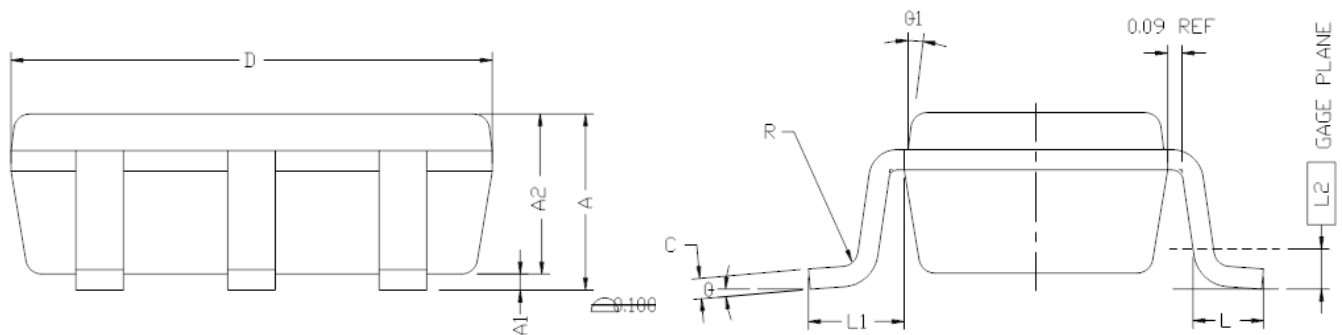
Typical Electrical Characteristics



## Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	---	1.10
A1	0.01	---	0.10
A2	0.925	---	1.00
b	0.25	0.32	0.40
c	0.10	0.15	0.20
D	2.95	3.05	3.10
E	2.70	2.85	2.98
E1	1.55	1.65	1.70
e	0.95 BSC		
L	0.30	---	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
theta	0?	4?	8?
theta1	7? NOM		



## Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.