

N-Channel 30-V (D-S) MOSFET

Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

Typical Applications:

- Power Routing
- Li Ion Battery Packs
- Level Shifting and Driver Circuits

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
30	15 @ $V_{GS} = 4.5V$	7.7
	23 @ $V_{GS} = 2.5V$	6.2

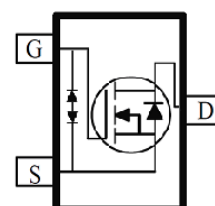
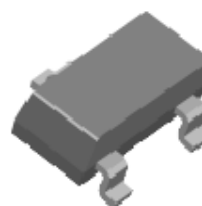
SOT-23



RoHS
COMPLIANT
HALOGEN
FREE



ESD Protected



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	7.7
	$T_A = 70^\circ\text{C}$		6
Pulsed Drain Current ^b	I_{DM}	30	A
Continuous Source Current (Diode Conduction) ^a	I_S	2.2	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.3
	$T_A = 70^\circ\text{C}$		0.8
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	$t \leq 10 \text{ sec}$	100
		Steady State	166

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Electrical Characteristics

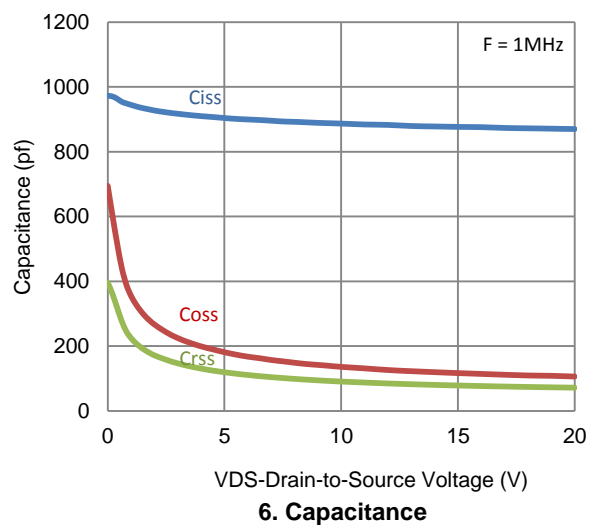
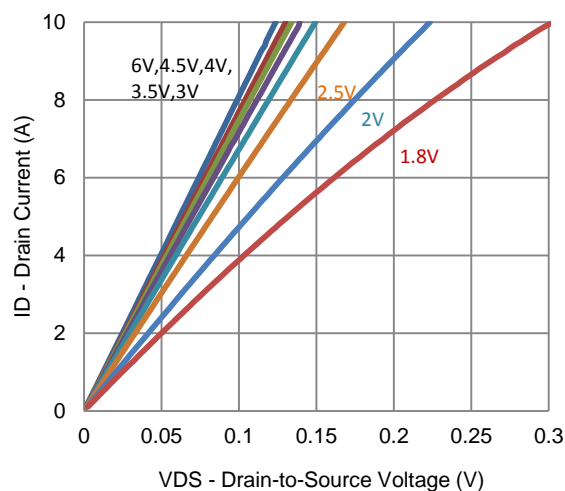
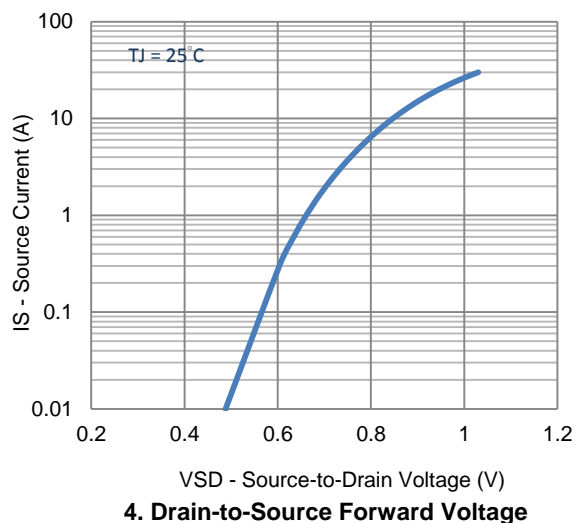
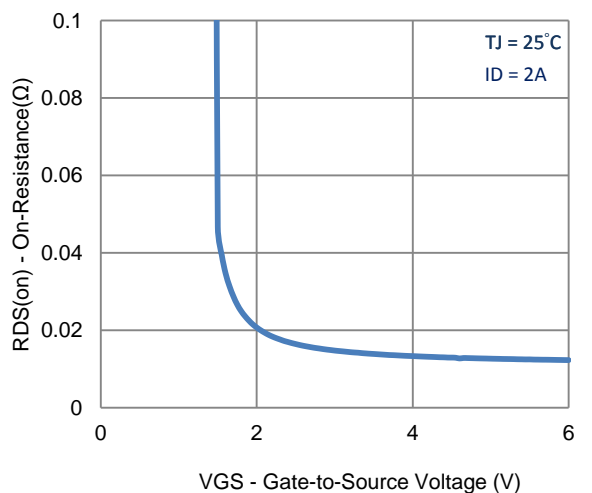
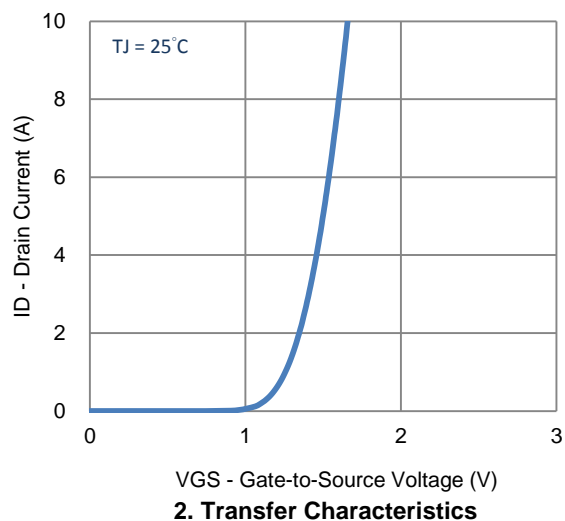
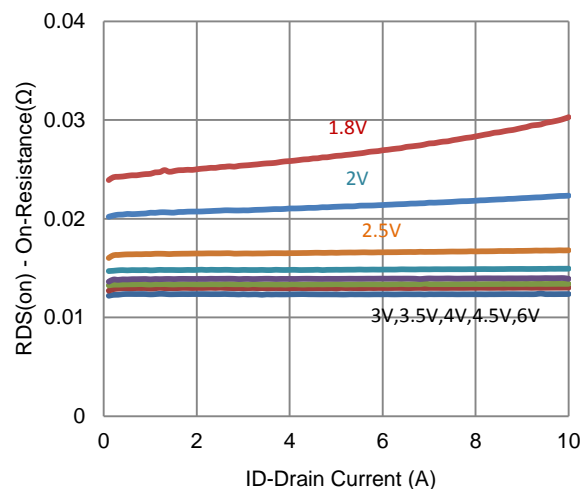
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.5			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 10	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$			1	μA
		$V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55^\circ C$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 4.5 V$	10			A
Drain-Source On-Resistance ^a	$r_{DS(on)}$	$V_{GS} = 4.5 V, I_D = 2 A$			15	m Ω
		$V_{GS} = 2.5 V, I_D = 1.6 A$			23	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 V, I_D = 2 A$		3		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.1 A, V_{GS} = 0 V$		0.68		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 15 V, V_{GS} = 4.5 V,$ $I_D = 2 A$		19		nC
Gate-Source Charge	Q_{gs}			2.9		
Gate-Drain Charge	Q_{gd}			6.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 15 V, R_L = 7.5 \Omega,$ $I_D = 2 A,$ $V_{GEN} = 4.5 V, R_{GEN} = 6 \Omega$		0.3		μs
Rise Time	t_r			0.6		
Turn-Off Delay Time	$t_{d(off)}$			3.9		
Fall Time	t_f			1.6		
Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 \text{ Mhz}$		876		pF
Output Capacitance	C_{oss}			116		
Reverse Transfer Capacitance	C_{rss}			78		

Notes

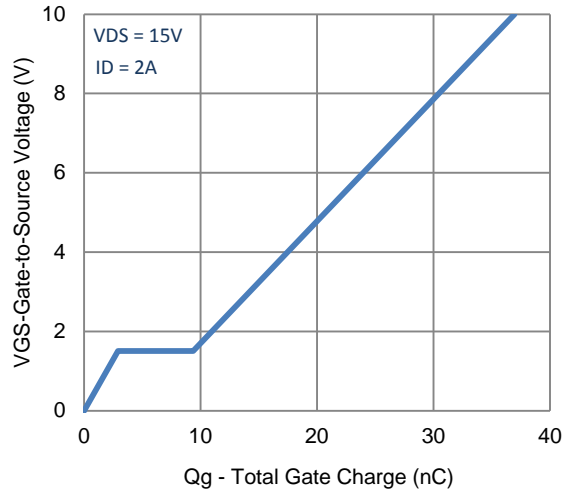
- a. Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

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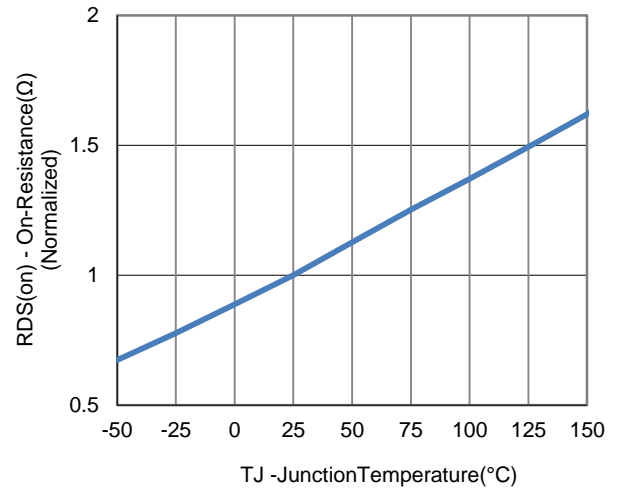
Typical Electrical Characteristics



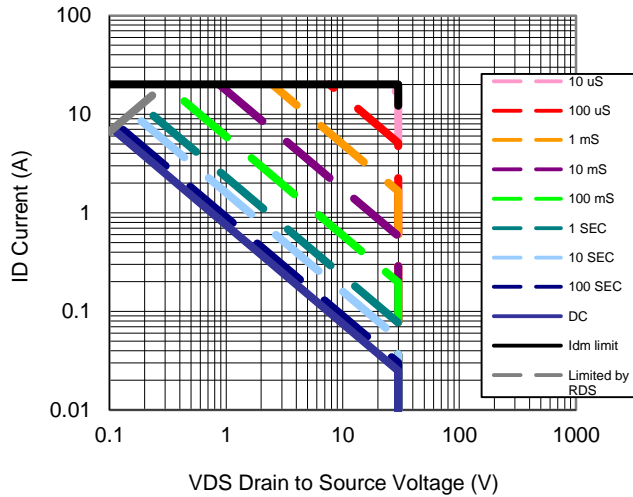
Typical Electrical Characteristics



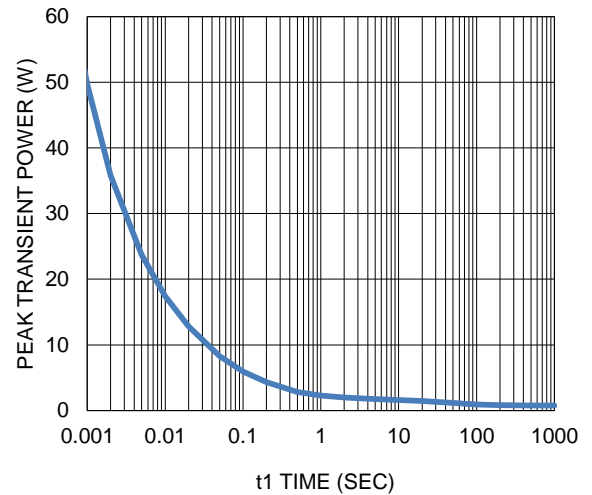
7. Gate Charge



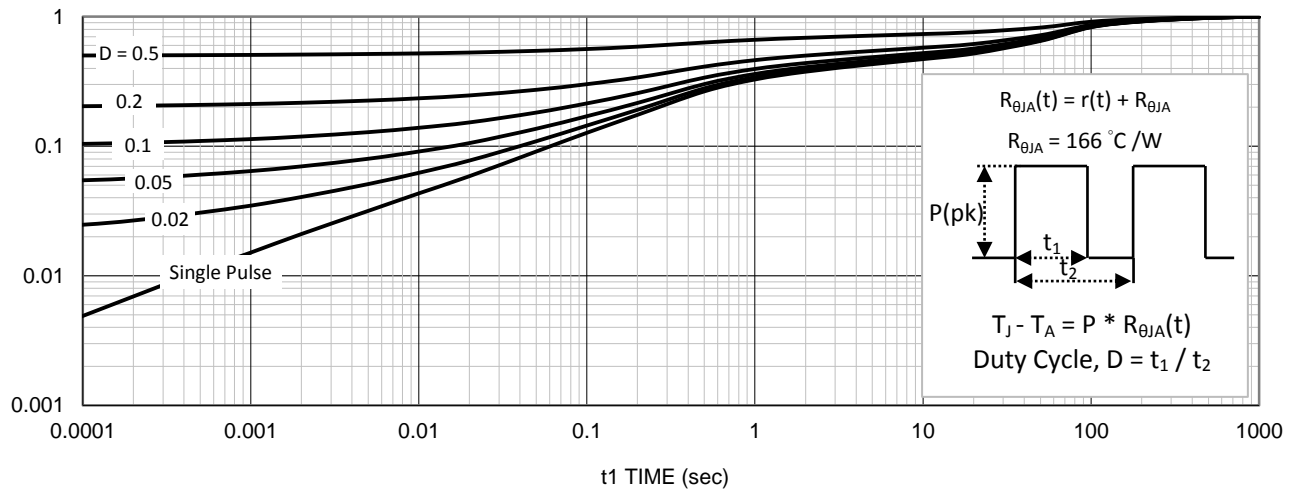
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

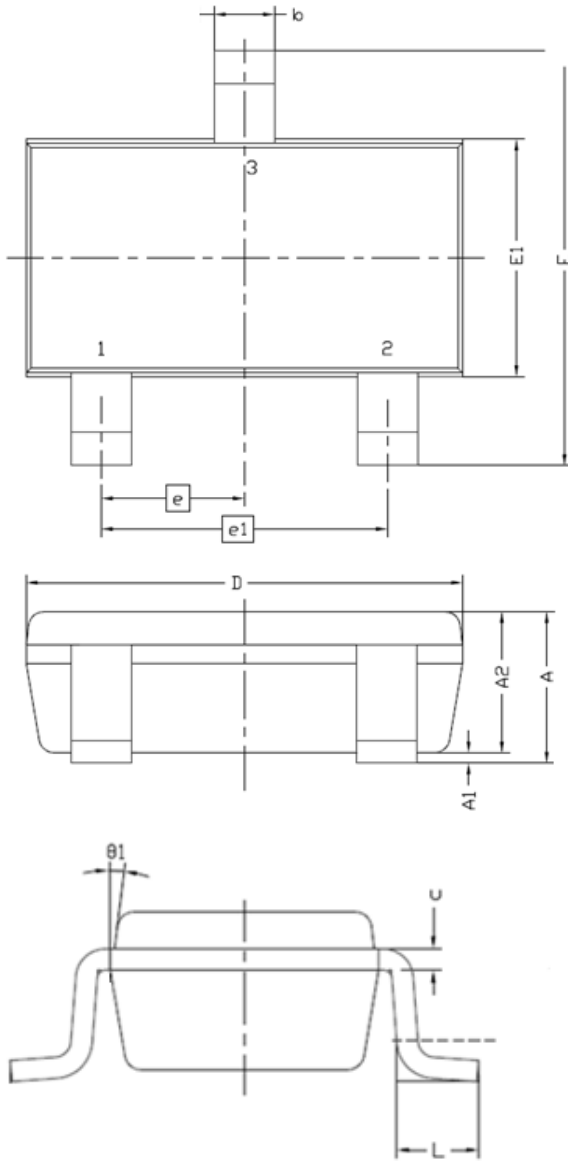


10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

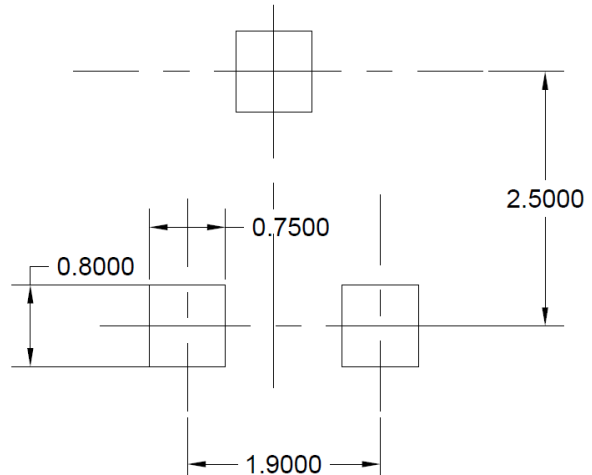
Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout

Note: Drain opening is recommended to be solder mask defined in a copper fill to provide improved thermal performance



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