Analog Power

P-Channel 20-V (D-S) MOSFET

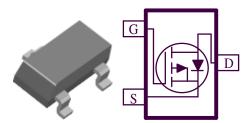
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY				
V _{DS} (V)	$I_{\rm DS(on)} (\rm OHM) \qquad I_{\rm D} (\rm OHM)$			
20	$0.130 @ V_{GS} = -4.5V$	-2.6		
-20	$0.190 @ V_{GS} = -2.5V$	-2.1		

ESD Protected



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	Maximum	Units		
Drain-Source Voltage		V _{DS}	-20	v		
Gate-Source Voltage		V _{GS}	±8	v		
Continuous Drain Current ^a	T _A =25°C	T_	-2.6			
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ъD	-1.5	А		
Pulsed Drain Current ^b		I _{DM}	-10			
Continuous Source Current (Diode Conduction) ^a		Is	±1.6	А		
	T _A =25°C	D_	1.25	W		
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	гD	0.8	vv		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
Maximum Junction-to-Ambient ^a	t <= 5 sec	B	100	°C/W	
	Steady-State	R_{THJA}	166	C/W	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Demonster	S-mah - 1		Limits			.	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_D=-250uA$	-0.4		-1		
Gate-Body Leakage	Igss	$V_{DS} = 0 V, V_{GS} = +/-8 V$			±10	μA	
Zana Cata Valta ao Duain Cumant	I	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA	
Zero Gate Voltage Drain Current	Idss	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}C$			-10		
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = -5 V$, $V_{GS} = -4.5 V$	-3			Α	
	r _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -1 \text{ A}$			0.130	Ω	
Drain-Source On-Resistance ^A		$V_{GS} = -2.5 \text{ V}, I_D = -1 \text{ A}$			0.190		
Forward Tranconductance ^A	g _{fs}	$V_{DS} = -5 V, I_D = -1 A$		3		S	
Diode Forward Voltage	V _{SD}	$I_S = -1 A, V_{GS} = 0 V$		-0.70		V	
Dynamic ^b							
Total Gate Charge	Qg	$V_{DS} = -5 V$, $V_{GS} = -4.5 V$,		3		nC	
Gate-Source Charge	Qgs	$v_{DS} = -3 v, v_{GS} = -4.3 v,$ ID = -1 A		0.6			
Gate-Drain Charge	Qgd	ID = -1 A		0.9			
Turn-On Delay Time	t _{d(on)}			9	_	ns	
Rise Time	tr	$V_{DD} = -5 \text{ V}, \text{R}_L = 5 \text{ OHM},$		10			
Turn-Off Delay Time	t _{d(off)}	$V_{\rm GEN}$ = -4.5 V, $R_{\rm G}$ = 6 OHM		30			
Fall-Time	t _f	1		10			

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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Package Information

