

## P-Channel 200-V (D-S) MOSFET

### Key Features:

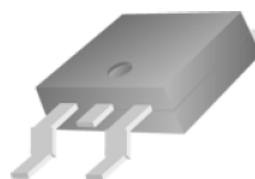
- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed

### Typical Applications:

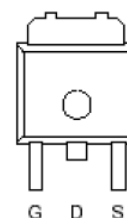
- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



TO-252



Top View

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
-200	200 @ $V_{GS} = -10V$	-20 <sup>a</sup>
	210 @ $V_{GS} = -6.5V$	

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		$V_{DS}$	-200	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$T_C = 25^\circ\text{C}$	$I_D$	-20	A
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	-80	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-20	A
Power Dissipation <sup>a</sup>	$T_C = 25^\circ\text{C}$	$P_D$	50	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	40	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3	

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

## Electrical Characteristics

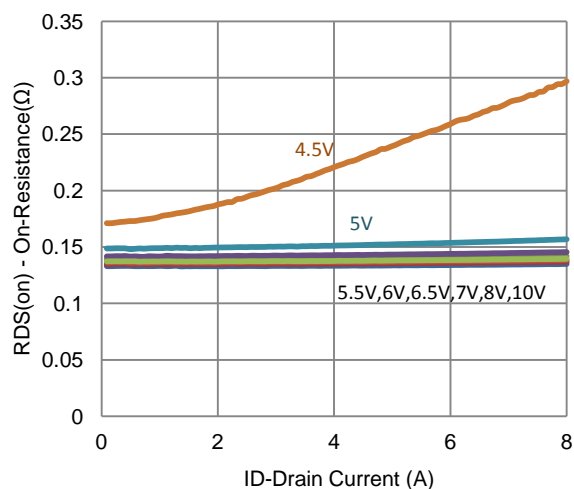
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -160 V, V_{GS} = 0 V$			-1	$\mu A$
		$V_{DS} = -160 V, V_{GS} = 0 V, T_J = 55^\circ C$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5 V, V_{GS} = -10 V$	-25			A
Drain-Source On-Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10 V, I_D = -8 A$			200	m $\Omega$
		$V_{GS} = -6.5 V, I_D = -6.4 A$			210	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -50 V, I_D = -8 A$		22		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -10 A, V_{GS} = 0 V$		-0.87		V
<b>Dynamic <sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -100 V, V_{GS} = -6.5 V,$ $I_D = -1 A$		64		nC
Gate-Source Charge	$Q_{gs}$			21		
Gate-Drain Charge	$Q_{gd}$			24		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = -100 V, R_L = 100 \Omega,$ $I_D = -1 A,$ $V_{GEN} = -10 V, R_{GEN} = 6 \Omega$		16		ns
Rise Time	$t_r$			20		
Turn-Off Delay Time	$t_{d(off)}$			95		
Fall Time	$t_f$			57		
Input Capacitance	$C_{iss}$	$V_{DS} = -50 V, V_{GS} = 0 V, f = 1 \text{ Mhz}$		2799		pF
Output Capacitance	$C_{oss}$			78		
Reverse Transfer Capacitance	$C_{rss}$			77		

## Notes

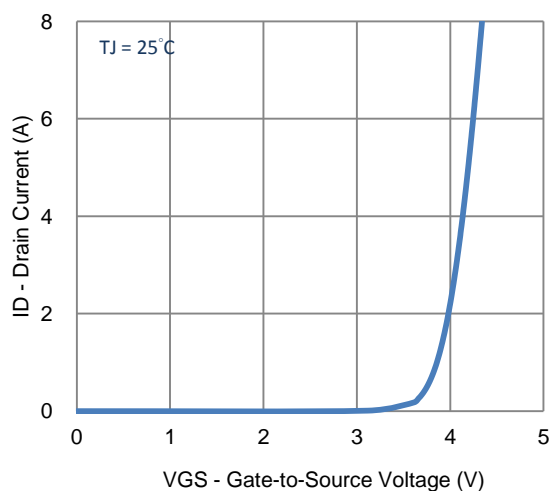
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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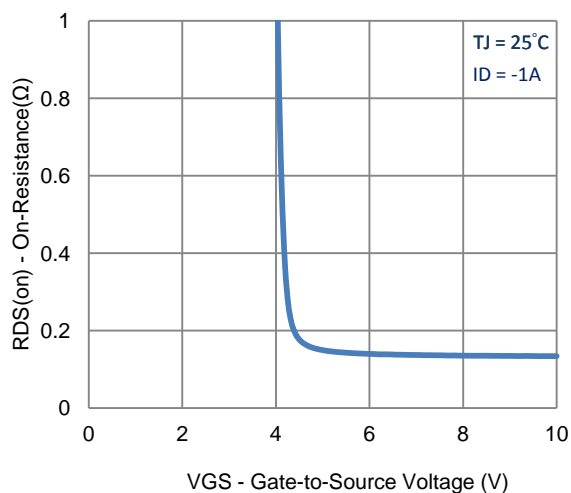
## Typical Electrical Characteristics



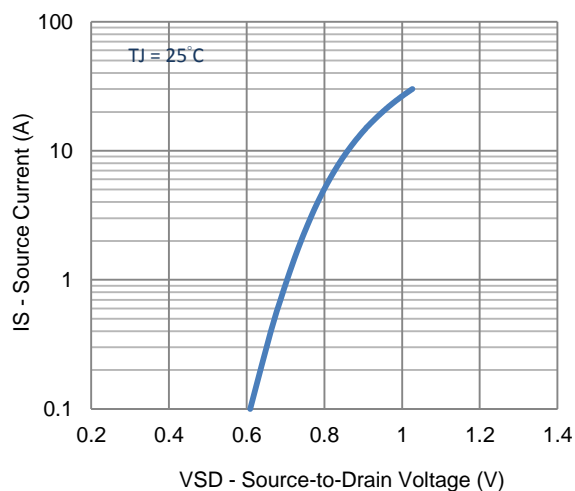
1. On-Resistance vs. Drain Current



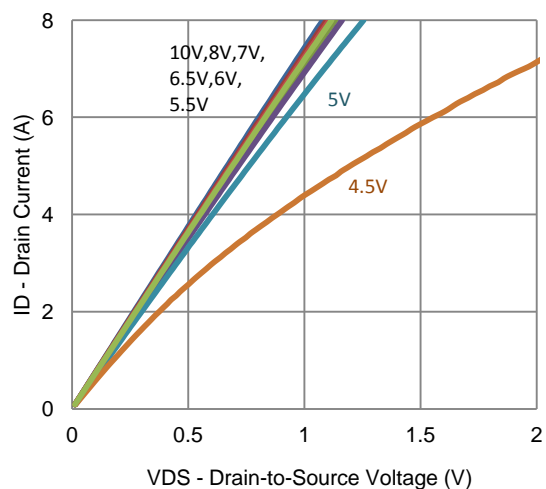
2. Transfer Characteristics



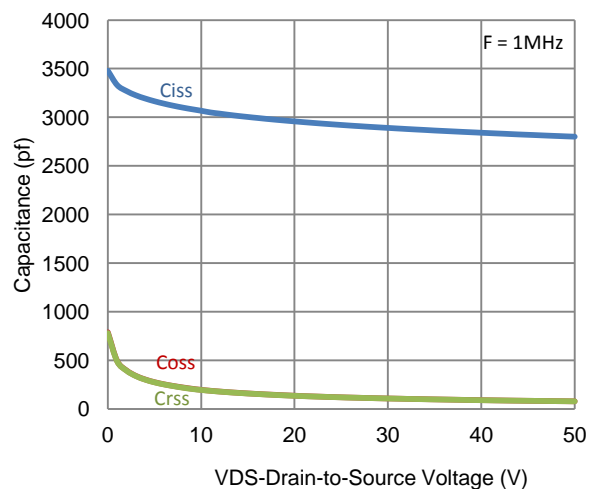
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

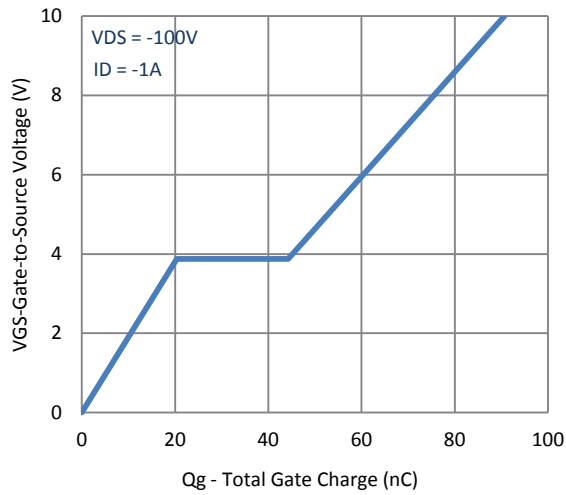


5. Output Characteristics

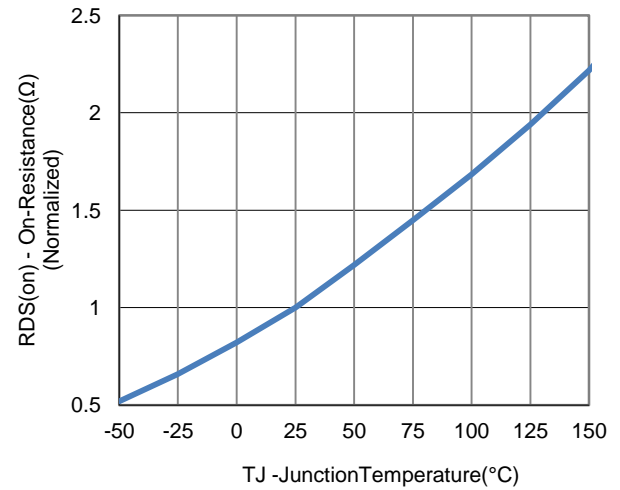


6. Capacitance

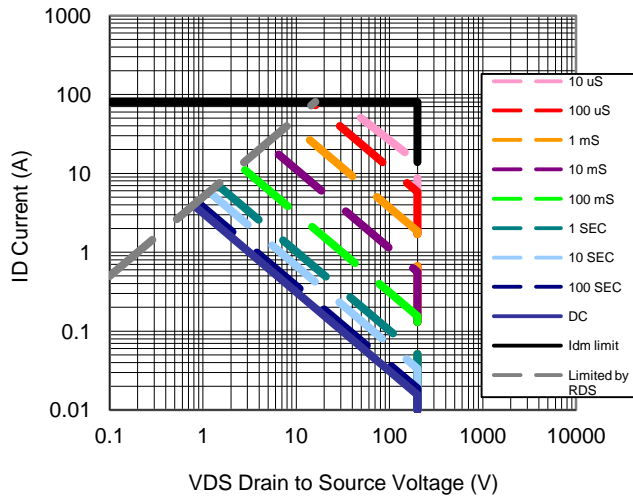
## Typical Electrical Characteristics



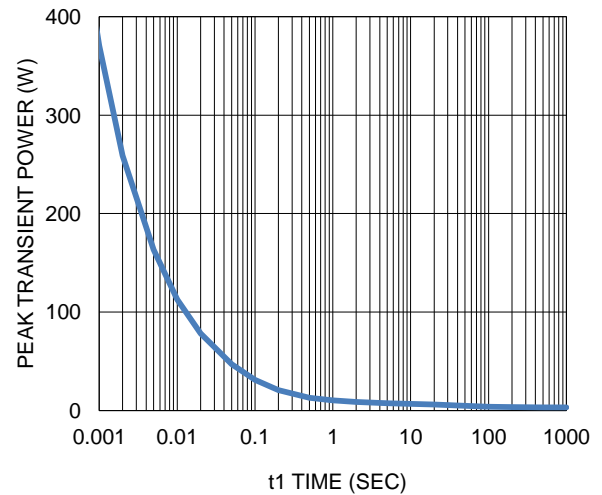
7. Gate Charge



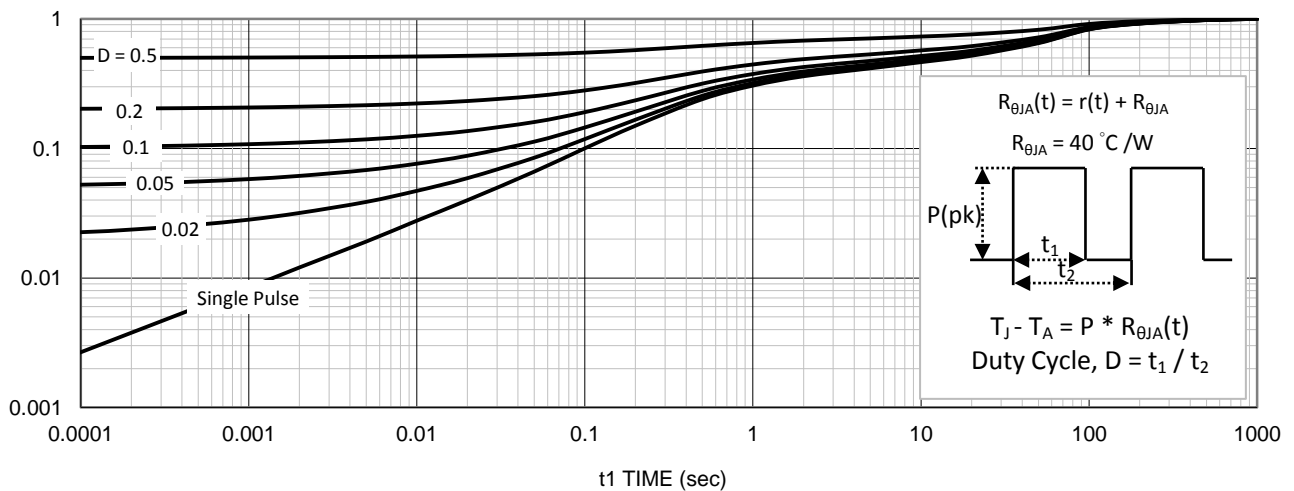
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

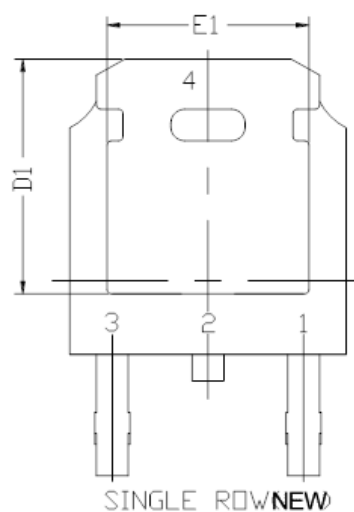
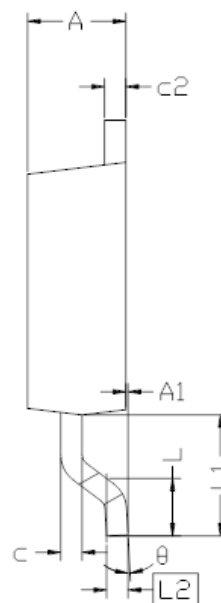
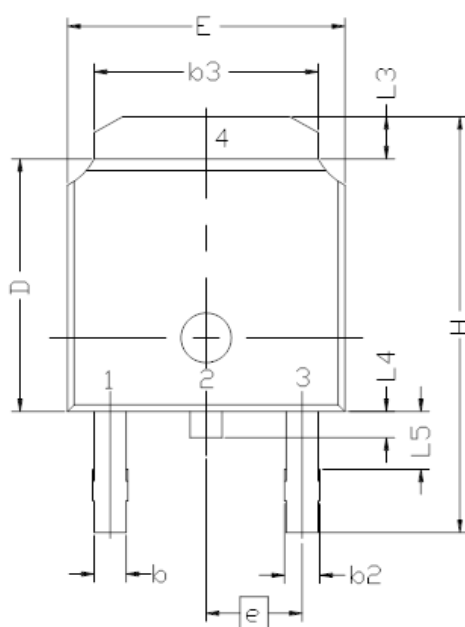


10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

## Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.30	--	--
E1	4.40	--	--
θ	0°	--	10°

## Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.