Analog Power

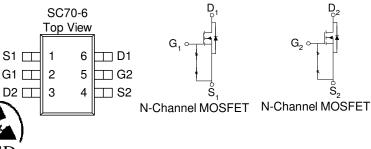
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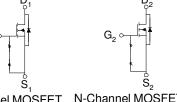
N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe S1 SC70-6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY					
V _{DS} (V)	$\mathbf{r}_{\mathrm{DS(on)}}\left(\mathbf{m}\mathbf{\Omega} ight)$	I _D (A)			
20	88 @ $V_{GS} = 4.5V$	1.6			
	$120 @ V_{GS} = 2.5V$	1.3			





ABSOLUTE MAXIMUM RATINGS (TA = 25 °C UNLESS OTHERWISE NOTED)										
Parameter				l Maximum	Units					
Drain-Source Voltage				20	v					
Gate-Source Voltage				8	v					
Continuous Drain Current ^a		T _A =25°	C	1.6						
		$T_{A}=25^{\circ}$ $T_{A}=70^{\circ}$	C	1.3	А					
Pulsed Drain Current ^b				5						
Continuous Source Current (Diode Conduction) ^a				0.4	А					
Power Dissipation ^a		$\frac{T_{A}=25^{\circ}C}{T_{A}=70^{\circ}C}P_{D}$		0.3	W					
		$T_A=70^\circ$	C	0.21	VV					
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to 150	°C					
THERMAL RESISTANCE RATI	NGS		-							
Parameter			Symbol	Maximum	Units					
Maximum Junction-to-Ambient ^a	t <= 5 sec		R _{THJA}	415	°C/W					
	Stead	y-State	1115/1	460	C/ W					

Protected

Notes

Surface Mounted on 1" x 1" FR4 Board. a.

Pulse width limited by maximum junction temperature b.

Domorrotor			Limits			T T •4
Parameter	Symbol	Test Conditions		Тур	Max	Unit
Static	_					
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \text{ uA}$	0.3			V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			±25	uA
Zana Cata Valta a Duain Comunit	т	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			5	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 V, V_{GS} = 4.5 V$	2			Α
Drain-Source On-Resistance ^A	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 0.3 \text{ A}$			88	mΩ
Drain-Source On-Resistance		$V_{GS} = 2.5 \text{ V}, I_D = 0.2 \text{ A}$			120	
Forward Tranconductance ^A	$g_{\rm fs}$	$V_{DS} = 4.5 \text{ V}, I_D = 0.3 \text{ A}$		8		S
Diode Forward Voltage	V _{SD}	$I_{s} = 0.2 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
Dynamic ^b						
Total Gate Charge	Qg			1		
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 0.3 \text{ A}$		0.4		nC
Gate-Drain Charge	Q _{gd}			0.6		Î
Turn-On Delay Time	t _{d(on)}			7		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, R_{L} = 30 \Omega, \qquad I_{D} = 0.3 \text{ A}, V_{GEN} = 10 \text{ V}$		14		ns
Turn-Off Delay Time	t _{d(off)}			25		
Fall-Time	t _f			10		Ī

Notes

- a. Pulse test: $PW \le 300$ us duty cycle $\le 2\%$.
- b. Guaranteed by design, not subject to production testing.

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