Analog Power

P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low r_{DS(on)} provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-6 saves board space
- Fast switching speed
- High performance trench technology

	PRODUCT SUMMARY							
	VD	s (V)	r _{DS(on)} (OHM)			$I_D(A)$		
		20	0.0)79 @V	-3.7			
		-20		110@	$V_{CS} = -2.5V$	-3.1		
	SC70-6 S							
	Top View			7	C			
D		1	6	D D	G			
D		2	5	D 🗗	c			
G		3	4	⊨ s	C)		
				l	P-Channel	MOSFET		

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Maximum	Units				
Drain-Source Voltage	V _{DS}	-20	V				
Gate-Source Voltage	V _{cs}	±8	v				
Continuous Drain Current ^a	$T_A=25^{\circ}C$	T_	-3.7				
	T _A =25°C T _A =70°C	ъD	-3.0	Α			
Pulsed Drain Current ^b			-10				
Continuous Source Current (Diode Conduction) ^a		Is	±1.4	Α			
	$T_A=25^{\circ}C$	D_	1.56	W			
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	тD	0.81	vv			
Operating Junction and Storage Temperature Range			-55 to 150	°C			

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Maximum	Units			
	$t \ll 5 \sec$	R _{THJA}	80	°C/W			
Maximum Junction-to-Ambient ^a	Steady-State		125				

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Description	G		Limits			.
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Gate-Threshold Voltage	VGS(th)	$V_{DS} = V_{GS}$, ID = -250 uA	-0.4			V
Gate-Body Leakage	IGSS	$V_{DS} = 0 V, V_{CS} = \pm 8 V$			±100	nA
Zom Cata Valtaga Dain Gumant	Ipss	$V_{DS} = -16 V, V_{GS} = 0 V$			-1	– uA
Zero Gate Voltage Drain Current	IDSS	V_{DS} =-16 V, V_{CS} =0 V, T_J =55°C			-10	uA
On-State Drain Current ^A	ate Drain Current ^A $I_{D(on)}$ $V_{DS} = -5 V_2 V_{CS} = -4.$		-5			Α
		V_{GS} = -4.5 V, I_D = -3.7 A			79	
Drain-Source On-Resistance ^A	rDS(on)	$V_{GS} = -2.5 V$, ID = -3.1 A			110	mΩ
Forward Tranconductance ^A	gś	$V_{DS} = -5 V$, ID = -1.25 A		9		S
Diode Forward Voltage	Vsd	$I_{\rm S}$ =-0.46 A, $V_{\rm GS}$ =0 V		-0.65		V
Dynamic ^b						
Total Gate Charge	Qg	$X_{} = 10 X X_{} = 45 X$		7.2		
Gate-Source Charge	Qgs	$V_{DS} = -10 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V},$ $I_{D} = -3.7 \text{ A}$		1.7		nC
Gate-Drain Charge	Qgd	1D3./A		1.5		
Tum-On Delay Time	td(on)			10		
Rise Time	tr	V_{DD} =-10 V, I _L =-1 A,		9		120
Tum-Off Delay Time	td(off)	$V_{\text{GEN}} = -4.5 \text{ V}, \text{R}_{\text{G}} = 6 \Omega$		27		ns
Fall-Time	tſ			11		

Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Repetitive rating, pulse width limited by junction temperature.

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